User manual

Computer Controlled Teletext

COMPUTER CONTROLLED TELETEXT

USER'S MANUAL

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Introduction

This document describes the operation and use of the EURO CCT Computer Controlled Teletext integrated circuit SAA5240. System configurations are described using the device together with the VIP2 Video Processor circuit SAA5230 and other components to give various types of teletext and viewdata decoders.

Although this document gives a functional description of the device, it is not a specification. The electrical parameters of the chip are given in the System Specification.

As a computer controlled system, this document describes the commands necessary to perform various functions. It does not, however, give examples of control software listings. A range of software packages for different applications will be prepared, and will be described separately. For those wishing to write their own software, this user's manual should contain sufficient information on the operation of the device.

Information on evaluation kits is issued separately, together with the associated software descriptions.

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1 General System Philosophy

This section describes the design approach used for EURO CCT, and outlines the features and flexibility of the system. Most readers will be familiar with the first-generation LSI teletext decoder, so this is taken as a starting point to explain how the EURO CCT decoder design was devised.

1.1 The first-generation LSI decoder

A block diagram of the first-generation LSI teletext decoder is shown in fig.1. Within the decoder board itself are the following integrated circuits:

* VIP (Video Input Processor) (SAA 5030), a bipolar linear device which provides serial data and clock derived from the incoming video signal; it also arranges timing synchronisation for the rest of the decoder.

* TAC (Teletext data Acquistion and Control) (SAA 5040), a digital NMOS device which arranges the capture of the requested page into memory. It is also concerned with overall decoder control, and writing user status into memory.

* RAM 1k8 of memory for page storage (e.g. 2*2114)

* TROM (Character generator) (SAA 5050), an NMOS device containing a ROM for generating characters from a dot matrix, and other control functions.

* TIC (Timing chain) (SAA 5020), an NMOS device providing timing and addressing signals for the whole decoder.

* RAM interface, usually 4 standard LSTTL circuits to interface the page memory.

Also shown in fig.1 is the remote control system, consisting of a keyboard and transmitter device within the hand held circuit and an infra - red link to the remote control decoder device within the t.v. set or adapter. Although these parts are not normally on the teletext decoder board they must be considered to be an integral part of the design.

It will be noted that the decoder design contains no programmable elements; the function of the decoder is fixed in hardware. A lot of the system problems are solved for the customer using this approach, but it does mean that its flexibilty is limited. In fact a number of device variants are produced for different requirements, notably TACs for different status and user control, and TROMs for different languages.

1.2 Improving Decoder Flexibility and Performance

When the functions of a teletext decoder are analysed,it can be seen that they fall broadly into two categories. Firstly, there are functions which are fixed by the broadcast specification and always need to be performed in much the same way. Examples are data slicing, timing and sync. generation. The second category covers functions which are likely to change significantly between different customers and applications, for example response of the decoder to different command keys, on-screen status messages and displayed languages. These kind of features need to be programmable if a number of different applications are to be done well.

The philosphy behind the EURO CCT-based teletext decoder is that the fixed functions should be done in the best and most economical way using dedicated circuitry in the integrated circuits. The most cost-effective approach for the variable functions is to do them in software in an associated control microcomputer. This gives rise to the name, EURO CCT : European (i.e 625 line) Computer Controlled Teletext.

Other factors need to be considered in the design of a second-generation teletext decoder. Some of the more important ones will be mentioned here, but there are many other detailed points which will be found under the relevant sections.

Since the first-generation decoder was designed in 1976 i.c. technology has made great progress and some improvements to the basic decoder performance are now possible. In terms of data capture a new Video Input Processor device VIP2 (SAA5230) has been designed with better performance under poor signal conditions. For full details see the VIP2 documentation. On the display side, it is now possible to provide a non-interlaced display without flicker problems, while at the same time capturing data from an interlaced T.V. transmission. A major improvement in character shape can also be achieved, using a 12 x 10 dot resolution ROM in place of the original 5 x 9.

The potential of the teletext system as a whole has also moved forward with the definition of a fully-compatible multi-level specification (reference 1). This provides for a range of system performances (and costs) from the established level 1 up to level 5 with sophisticated graphics, pastel colours etc. While the display facilities of EURO CCT remain basically at level 1 on grounds of cost it is possible to capture data for all levels. This allows advantage to be taken of such features as linked pages, automatic language switching, programme service rows, telesoftware etc. when sufficient extra resources are built into the decoder.

Another feature of EURO CCT which may become important is the ability to capture data in full channel mode, i.e. with teletext data on all t.v. lines. This allows a large data transfer rate (>600 pages/second) on a dedicated channel which may be useful for satellite or cable t.v. systems, or even simple data distribution networks.

From the users point of view, access time to the required page is of paramount importance and EURO CCT's ability to search for four pages simultaneously could come in useful. Also more helpful status messages, on a separate row from the main text, may be generated.

As a mass-market consumer product, the major factor to be borne in mind is the question of cost. Clearly it is the total cost of the decoder within a t.v. set or adaptor that must be considered, not just the price of the integrated circuits. A EURO CCT based teletext decoder can be built on a single sided printed circuit board, and indeed many setmakers may decide to incorporate the decoder into the main t.v. circuit board to reduce costs. One of the principles governing the EURO CCT decoder was that more complex and sophisticated systems should be possible by adding extra resources (hardware and software), while maintaining a low cost for the simple basic decoder. The extent to which these objectives have been achieved may be judged from the following pages.

1.3. The EURO CCT-based Decoder.

A block diagram of the EURO CCT-based decoder is shown in fig. 2. This is a 'standard' single page decoder which may be compared directly with the first-generation LSI decoder in fig.1.

The video processing function (data slicing, clock regeneration, timing synchronisation) remains in the bipolar linear device VIP2. However two small circuits (the field sync integrator and signal quality detector) are no longer included, so VIP2 is not an exact replacement for VIP1. These functions are now performed digitally inside EURO CCT.

The acquisition, timing, character generation and memory interface functions of the decoder are all performed inside EURO CCT. This single 40 pin circuit is therefore effectively a replacement for seven i.c.'s in the first-generation LSI decoder - TAC, TIC, TROM, and the four TTL interface circuits. EURO CCT does not include, however, the remote control command processing and status functions, formerly carried out in TAC. These are required to be programmable and so are performed in the control micro-computer.

Standard static RAM is connected to EURO CCT as page memory. For a single page decoder 1K bytes are required (1K8), but up to 8K bytes may be connected.

The control microcomputer is used to decode the remote control pulses from the infrared receiver. It also controls the operation of the decoder, and provides status messages. Depending on the particular application, the micro-computer may also control other t.v. functions such as a tuning system, or may be dedicated to controlling the teletext decoder.

The interface beween the microcomputer and EURO CCT is the standard IIC (inter integrated circuit) bus. Although most data flow is from the micro-computer to EURO CCT, the bus is bidirectional so that, for example, data in the page memory may be read by the microcomputer.

1.4. EURO CCT Functions and Pinning.

A simpified block diagram of EURO CCT is shown in fig.3. There are five major functions performed in EURO CCT: Timing Chain, Character Generator, Data Acquisition, Memory Interface and IIC Interface and Control. Each of these is described in detail in the sections which follow.

Briefly, serial data and clock signals from VIP2 are input through the TTD and TTC pins and the appropriate data is captured by the Data Acquisition function. It is then passed on to the RAM via the Memory Interface. Data is read from the RAM via the Memory Interface and supplied to the Character Generator, which in turn provides R,G,B, drive outputs for the video stages of the t.v. set (or a modulator in the case of an adaptor). Outputs are also provided for blanking and contrast reduction of the t.v. picture (BLAN and $\overline{COR}$), together with a monochrome text signal for driving a printer (Y).

The Memory Interface has 8 parallel data input/outputs (D0.....D7) and 13 address outputs (A0.....A12) which interface up to 8K bytes of static RAM. Control signals $\overline{OE}$ (output enable) and $\overline{WE}$ (write enable) are also provided . The RAM cycle is 500ns, with in general one write and one read cycle every microsecond.

Timing signals for the whole circuit are provided by the Timing Chain function, which operates from a 6MHz clock F6 from VIP2. Line synchronisation with the incoming signal is performed by a phase locked oscillator in VIP2, which is provided with a reference signal SAND from EURO CCT. A composite sync. waveform VCS from VIP2 provides field synchronisation for the acquisition timing, and also the display timing when interlaced display is selected. The display timing circuit generates a composite sync. waveform TCS which is used to drive the display timebases via VIP2; alternatively the pin can be made an input and driven by a composite sync. waveform to 'slave' the display timing circuits.

The IIC Interface and Control section provides the means for controlling the variable functions of EURO CCT, either directly using mode register bits or indirectly via the memory devices. The IIC bus slave transceiver accepts commands from the microcomputer via the SDA and SCL (serial data and clock) pins.

EURO CCT is operated by a single 5V supply, the common earth pin being Vss and +5V pin is Vdd.

The pinning diagram of EURO CCTis shown in fig.4.

2. System Configurations

This section describes a number of ways in which EURO CCT can be used with other devices to produce different types of decoder. More general design considerations and interfacing aspects are covered here.

2.1. Basic Single Page Decoder

The circuit diagram of a basic single page teletext decoder, as built into a t.v. receiver, is shown in fig. 5. There are two main sections:

* The decoder board itself, incorporating VIP2, EURO CCT, RAM and interface circuits.

* The remote control system, comprising the keypad, transmitter, infra-red link, amplifier and control microcomputer.

In many cases these two sections will be physically separate, with relatively long interconnecting lines. Flashover protection components are essential in this environment and are indicated by * in fig. 5. If the two sections are built together on a common board the flashover protection components may be omitted.

The interconnections around the microcomputer assume it has control of the teletext decoder only, but in many cases it will be used for more general t.v. control functions. Pressing a button on the keypad activates the transmitter, which pulse modulates the infra-red link. The received signal is amplified and presented to the interrupt pin on the microcomputer, thus activating a software routine for decoding the command. Further software in the microcomputer decides the action to be taken in that case and sends an IIC bus command as appropriate down the SDA and SCL lines.

One control function to the teletext decoder is not performed via the IIC bus; this is the $\overline{VCR}$ mode signal to VIP2. The object of this function is to shorten the time constants of the display phase locked loop when a video tape recorder input is selected, so that stable status displays are obtained in spite of timing jitter from the video tape recorder. The $\overline{VCR}$ line to VIP2 is shown coming from a port pin on the control microcomputer; however it may also be required by the line timebase in the t.v. set and could be derived, e.g. from the tuning system.

Input video from the demodulator of the set is coupled to the CV (Composite Video) pin on VIP2. The data slicing function in VIP2 generates serial data TTD and data clock TTC which are passed to EURO CCT. The composite sync part of the video signal is output as VCS, and its line component is compared with SAND to provide the phase locked 6MHz system clock F6. The $\overline{TCS}$ output from EURO CCT is passed through VIP2 to the STTV pin, which provides the sync signal to the t.v. receiver timebases. Either polarity of output may be chosen depending on the connection of the load resistor. The $\overline{TCS}$ output of EURO CCT may be switched off under IIC bus command; when this happens VIP2 automatically provides composite video on the STTV pin, for synchronising a normal t.v. picture.

For detailed information on VIP2 peripheral components and features see the VIP2 documentation.

Interfacing of EURO CCT to the page memory is straightforward. A single page decoder uses 1k bytes of RAM, so ten of the address lines (A0 to A9) are sufficient. Eight data lines (D0 to D7) and two control lines, output enable ($\overline{OE}$) and write enable ($\overline{WE}$), complete the interface.

The output interface from the decoder to the video stages of the t.v. receiver depends on the t.v. design and the position of the decoder within it. However, the arrangement shown in fig. 5, which is designed to work with the TDA3560 PAL decoder circuit, is typical of the configuration required. The red, green and blue (R,G,B) outputs from EURO CCT are buffered by emitter followers and the upper voltage levels are clamped by the diodes to a potential which depends on the t.v. receiver's contrast control. With suitable component values this allows the text amplitude to follow the picture contrast, under a common control.

The blanking output (BLAN) is similarly buffered to give a switching signal for picture video. Note that with EURO CCT the BLAN pin provides full screen, box and dot blanking combined so there is no need for external OR-ing arrangements as used on the first-generation LSI decoder.

When the contrast reduce function is activated, the $\overline{COR}$ pin goes low. Using a suitable resistive network and diode this can be made to reduce the contrast voltage in the receiver by a preset amount. This can give more readable mixed displays, or subtitles in reduced contrast boxes for example.

Suitable decoupling capacitors (number and size depending on board layout) complete the single page decoder. The decoder shown in fig. 5 can occupy a single sided printed circuit board about 10cm square.

2.2. General Control Variations

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A type of decoder which may be required, at least in the short term, is a functional replacement for the first-generation LSI decoder. Such a decoder is shown in fig. 6.

All the components are on one board, and the major difference from the circuit of fig. 5 is the acceptance of MIBUS commands rather than infra-red pulses. Since the MIBUS signals are too fast for the microcomputer to deal with on a bit-by-bit basis, the MIBUS lines ($\overline{DATA}$ and DLIM) load an external shift register as well as driving the interrupt pin. On completion of the MIBUS command, the software loads the contents of the shift register into the microcomputer for analysis.

The normal control configuration, however, will be based on a common remote control decoding and teletext control microcomputer, as was shown in fig. 5. In some cases this microcomputer may also be responsible for the control of analogues and the tuning system. Fig. 7 shows an example of how the basic configuration might be extended to provide a comprehensive control system, including local keyboard control, display driving, memory for programmes and requested page numbers, etc.

All the examples shown here are based on the MAB8400 series of microcomputers. Available in a range of program memory sizes, they are particularly convenient to use in this kind of system because of the hardware serial bus interface provided on-chip. This greatly facilitates interfacing the IIC bus and the microcomputer can be programmed to act in a number of ways, e.g. master transmitter, slave receiver etc. It is important to realise that the IIC bus is a sophisticated interfacing technique which can support bidirectional data flow, multi-transmitter operation, data acknowledge, and data transfer rates up to 100kHz. For more details see section 7 and reference 2.

Some of the potential of this technique could be exploited in the kind of system shown in fig. 8. In this design a modular structure is used, with one microcomputer to perform the remote control decoding and tuning system drive functions and a second microcomputer dedicated to teletext decoder control. One common IIC bus connects both microcomputers, EURO CCT and the tuning chip (CITAC). Provided the remote control system has adequate resources in terms of numbers of keys (and 'transparent' software which sends out IIC commands for all keys), it is possible to add other systems at a later date (e.g. viewdata, VCR, cable decoder) simply by connecting to the common IIC bus.

Generally the IIC bus gives great flexibility in the design of systems and is convenient where sub-systems are physically some distance apart. In addition, an increasing number of special-purpose devices are being made with IIC bus interface on-chip. Examples are PCD8571, a 128 x 8 bit static CMOS RAM, PCB8573 clock/calendar chip, SAB3035 (CITAC) tuning and analogue control chip, and SAA1300 tuner switching circuit. Using these components it is possible to build sophisticated systems for all kinds of applications up to the limits of cost and the designer's imagination.

2.3. Multipage Decoders

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The great majority of teletext decoders produced to date have been single page, i.e. only one page is requested by the user at a time and subsequently displayed. EURO CCT makes possible the construction of a number of decoders with multipage capability, increasing the performance at extra cost.

The simplest way of providing multipage capability is to add a memory of requested page numbers. At any time the user can key in a list of favourite page numbers, which are stored in the extra memory. On switch-on, the control software can arrange for the decoder to look for the first requested page without any action on the part of the user. When the page has been read, the user presses a 'next page' key and the control software makes the decoder look for the second page in the list, and so on.

Although this method is very simple to implement (e.g. add one PCD8571 RAM on the IIC bus with extra control software to give 16 page requests) it does have a number of disadvantages. The major one is that it does nothing to reduce the access time, since each page is requested one at a time in the conventional manner. Also, the system tends to fossilise the page numbers accessed and discourage browsing through the magazines, which is not likely to endear it to the broadcasters (especially if advertisements are never accessed!).

A better way of achieving a multipage decoder is to search for several pages simultaneously. They are then all captured in one transmission cycle time, regardless of the order of transmission, and the access time apparent to the user is reduced. This, of course, requires extra page memory and a multipage acquisition circuit. EURO CCT is capable of searching for four pages simultaneously, and a four page decoder making use of this facility is shown in fig. 9.
A memory size of 4k bytes is required and extra software in the control microcomputer to deal with multipage requests. In a decoder such as this the control functions merit careful consideration, with suitable status displays to inform the user which pages are being requested and displayed. Probably the decoder would request pages on a cyclic basis (e.g. fifth page request overwrites first) with a 'next page' button, but of course the operation of the system would depend on the control software.

A variant on this type of decoder could be a system with 2k bytes of RAM when two pages are available. One of the memories would display the current page (and be kept updated by EURO CCT), while the other would be searching for the next requested page, either from a list in memory or by direct user input. When the 'next page' button was pressed, the memory functions would be reversed so that the new page was displayed and the old display memory used to search for the next page in the sequence. In view of the ready availability of 2k8 RAM devices at low cost this is likely to be a common configuration.

It is possible to connect up to 8 pages of memory to EURO CCT, but the acquisition circuit can search for only four pages simultaneously. This means that only four pages can be kept updated at a time. For more details of techniques to achieve an 8 page decoder see section 5.

Although the above examples of genuine multipage decoders are a real improvement in terms of solving access time problems, they do require more complex control. This may be a disadvantage in some applications and ways may be sought to improve the operating convenience of the decoder. Great advances in 'user-friendliness' can be achieved using the concept of ghost rows with linked pages.

Briefly, ghost rows can be transmitted in association with normal teletext pages, but they are invisible to the first-generation LSI decoders. Their objective is to provide completely compatible extensions to the teletext system and a multi-level specification to cater for the forseeable future has been devised (reference 1). Although the display facilities of EURO CCT are limited to level 1 of this specification, it is possible to capture data for all levels. If EURO CCT is switched by software command into ghost row mode, it can capture the ghost rows provided 2k bytes of memory are connected per page.

For a multipage decoder, the important ghost row is row 27, 'linked pages'. There can be up to four row 27's, each containing six page numbers (including sub-code). Thus each teletext page can have associated with it up to 24 other pages. There are two main ways in which these numbers can be used; branching and chaining. With branching, an index page contains the page numbers referred to in associated row 27's, allowing some form of short-code dialling to select them (e.g. 4th page instead of page number 117). When chaining, each page has a ghost row indicating the next page, previous page and index. This permits simple 'step forward' and 'step backward' buttons to be provided for the user, with no need for 3-digit page dialling. The order of page access is then predetermined by the broadcasters, but the pages are displayed when required by the user, giving a simple 'browsing' facility. Of course combinations and extensions of these methods can be used and with agreement on codes of practice by the broadcasters they can give simple user controls.

A four page decoder using ghost rows is shown in fig. 10. Apart from having 8k bytes of memory the hardware is the same as fig. 9, but of course more control software is required and the microcomputer is probably dedicated to decoder control.

2.4. Full Channel Decoders

The ability of EURO CCT to handle teletext data on all t.v. lines has already been mentioned. This is achieved using a software command to EURO CCT, and in general the hardware for a full channel decoder is the same as that required for normal field flyback mode. There is one minor difference, however, relating to page clearing.

When a page comes in for the first time, normally circuitry in EURO CCT arranges for the old data in the memory to be cleared out. This is no problem in field flyback mode as most of the field period is available for the clear function. However, with full channel mode wanted data may be coming in at the same time, so the clearing function is inhibited. There are two ways around this difficulty.

Firstly, the data base can be arranged to transmit non-row-adaptively, so that blank rows are always transmitted. There is then no need to clear the page as new data will overwrite the old. Alternatively, the page can be cleared by a command from the control software when a new page is requested, so that new data is received into an already blank memory. If the data base is very large, it is possible to arrange a second page of memory to display the old page until the new one has been received, thus avoiding a blank screen display. For further details see section 5.16.

2.5. Viewdata

The display standards of wired text systems are currently in transition to a higher level than teletext, with more sophisticated graphics, pastel colours, etc. However, the level 1 display available since the inception of e.g. the Prestel service is adequate for many applications at the lower cost end of the market and for these EURO CCT is an ideal display device.

For most viewdata systems the data rate is relatively low (e.g. 1200 baud) and this is easily transferred down the IIC bus into EURO CCT. In this way interfacing complexity is minimised. EURO CCT also contains facilities which facilitate the handling of the information, e.g. page clear command, automatic address increment and cursor display.

A viewdata-only terminal is shown in fig. 11. This consists of a MAB8440 microcomputer performing the decoding, connecting with SAA5070 (LUCY) and SAA5080 (LUCINDA) devices which interface the telephone line. The PCD8571 remembers telephone numbers for the autodialler and auto identification.

Another approach is to produce an add-on unit for viewdata to interface with the modular t.v. set architecture of fig. 8. Such a unit is shown in fig. 12, consisting of a microcomputer and telephone line interfacing components.

2.6. Telesoftware

The basic concept of telesoftware - transmitting computer programs via teletext - embraces a large variety of equipment and system configurations. If the application involves simple processing of alphanumeric data, for example, performing financial calculations, then the EURO CCT display facilities and transfer of data via the IIC bus would be adequate. This type of system could be built into a t.v. receiver as a more complex type of teletext decoder. with an additional microcomputer and perhaps more memory. Telesoftware protocols use the linked page facility to handle long programs and so EURO CCT would be operated in ghost row mode. If the keypad controls of the remote control system were sufficient for the application, a telesoftware add-on unit could be constructed for use with the modular t.v. system of fig. 8.

One difficulty with this approach is the data transfer rate via the IIC bus. At the maximum speed of 100kHz, a 'page' of 1k bytes of program would take about 100ms to transfer, with a similar time to build up the displayed page. These times may be considerably increased, however, if the IIC bus is common to other functions. In this case the bus is ocupied for other purposes, and its speed may have to be restricted for noise protection reasons. Also the time the microcomputer takes to process the data may be significant. Whether this is a problem or not depends on the application. Of course, the time taken to access the telesoftware data may be the dominant delay.

If data transfer rates through a common IIC bus are too slow, two possible solutions may be considered. The first is to have a dedicated IIC bus between EURO CCT and a telesoftware/decoder control microcomputer. Control signals to the system would come in via different pins on the microcomputer, thus allowing the dedicated IIC bus to go at full speed. Alternatively, data transfer could be arranged between the received data memory and the microcomputer using a parallel bus arrangement, allowing a much faster data rate. However, this requires additional hardware as the memory interface pins on EURO CCT cannot be disabled. Also it should be considered whether the interface should transfer data only when the memory has been filled, or in an interleaved mode when data is still being loaded into memory. The latter would require synchronising hardware to ensure there are no conflicts between memory write and read cycles.

For some applications a more sophisticated graphics display may be required. In these situations EURO CCT would be used as the telesoftware acquisition system, with a suitable form of interface to transfer the data to e.g. a home computer. It is also possible to use EURO CCT in "8-bit" mode (i.e. with normal parity checking disabled), allowing sophisticated error correctable or scrambled data streams to be dealt with for special applications.

The telesoftware technique could also be applied to page selection methods in sophisticated teletext decoders. This would allow a pseudo-interactive viewdata-like control scheme, by making the displayed page number depend on yes/no questions or selections. In view of the data base size this would be most applicable to full channel data systems.

It is also possible to think of telesoftware applications where a display is not required, for example a credit card verifier (with invalid card numbers transmitted by teletext). For these applications EURO CCT could still be a suitable acquisition-only device, in view of its multipage and ghost row capabilities.

2.7. Other Configurations

Although it is anticipated that the great majority of EURO CCT applications will have the device built into the same equipment as the display, it is also possible to construct adaptor units working into the aerial socket of a standard t.v. receiver. Part of such an adaptor is shown in fig. 13, which indicates how EURO CCT may be interfaced to the TEA1002 colour encoder circuit. Also required for a broadcast teletext adaptor are tuner, i.f. and demodulator circuits for the video input; together with a modulator for the output.

Teletext decoder 'peripherals' which may become important in the future include a page printer. This could either print teletext pages by user command, or automatically using pre-selected page numbers and sub-codes. There are two main ways of interfacing a printer. The first is to provide a real-time scanning dot stream from the Y output of EURO CCT, which is suitably buffered in the printer's electronics. Alternatively, character data can be read out of the display memory via the IIC bus and transferred to the printer, which in this case must have its own character generation system.

The same technique of reading character data through the IIC bus can also be applied to bulk storage of data, e.g. using a tape recorder. The IIC bus data is processed (and compressed, if necessary) by a micro-computer which drives a suitable modem function (e.g. part of LUCY SAA5070).

No doubt other configurations will occur to the system designer, but the examples shown in this section serve to illustrate the potential of this versatile device.

3 TIMING CHAIN FUNCTION

This section describes the timing chain function, which provides timing signals to all parts of the device. The digital signal quality detector is also included here. A block diagram of the timing chain function is shown in fig. 14.

3.1 Interface pins

The main 6MHz clock input to EURO CCT is applied to the F6 input pin. This clock, which will normally come from VIP2, is internally a.c. coupled and passed through a buffer circuit with feedback to give a 50% duty cycle.

Field synchronisation of EURO CCT is effected through the VCS input pin, which accepts a composite sync waveform from VIP2. This signal is also assessed by the signal quality detecter.

The SAND output of EURO CCT is a three-level signal, containing the phase lock (PL) and colour burst blanking (CBB) components for use in VIP2. The PL part of SAND is turned off under some circumstances to allow the VIP2 phase locked oscillator to free run.

The $\overline{TCS}/\overline{SCS}$ pin on EURO CCT is an input/output performing two functions. A text composite sync. output $\overline{TCS}$ can be provided for driving the display timebases , alternatively, a composite sync. input $\overline{SCS}$ (scan composite sync.) can be applied to give field synchronisation of the EURO CCT display timing (VIP2 provides line synchronisation).

Waveforms for these signals are shown in fig. 15.

3.2 Line rate timing

Referring to fig. 14, the buffered 6MHz clock from F6 is divided by six to produce a 1MHz clock signal. It is this clock which operates the majority of the two-phase dynamic logic on EURO CCT. Further division by 64 produces a number of line rate signals, which are derived from the associated decoder.

Two line rate signals, CBB and PL, are combined in the three level output SAND as mentioned earlier.The SAND signal is fed back to VIP2, which regenerates the PL signal and uses it as a reference to phase lock the F6 clock to the line synchronisation of the incoming video signal. In this way all the line rate timing signals in EURO CCT are phase locked to the broadcast.

Note that the line synchronisation of EURO CCT applies to both acquisition and display functions: they cannot be separated. It is therefore not possible, for example, to receive teletext data on one channel and at the same time display a subtitle on a t.v. picture coming from another channel.

If a free-running display system is acceptable and the acquisition circuit is not used (e.g. viewdata terminal) a fixed 6MHz clock can be applied to the F6 pin, the VCS pin earthed and the SAND pin not used.

When line synchronisation is required it is necessary to use SAND and a phase locked loop, as the line timing of EURO CCT cannot be reset. In most cases it will be simplest to use VIP2, even if the teletext acquisition function is not required.

The second part of SAND, CBB, is used in VIP2 to prevent the colour burst in the video waveform from interfering with the operation of the automatic data slicer. Other line rate signals are used in various parts of the ciruit and one of these provides count pulses to the acquisition line counter.

3.3 Acquisition timing chain

The acquisition line counter is a circuit which can divide by either 312 or 313 lines in response to a control signal. This signal comes from a divide by 2 odd/even field flip flop, which in turn is toggled as a result of a decode from the acquisition line counter. The whole combination acts a divide by 625 to count from line rate to frame rate.

A decode from the counter provides the internal data entry window (DEW) signal which is active during lines 6 to 22 inclusive in each field, i.e. lines 6 to 22 & 319 to 335.This is used by the acquisition circuit to determine when data can be accepted in normal field flyback mode.

The acquisition line counter and odd/even field flip flop are both reset by a valid field sync. edge occurring during the second half of the line. This is derived from the VCS composite sync. input by the digital field sync. integrator, so that only field sync. pulses at the end of an odd field /start of an even field are taken into account. The first field sync. pulse of this sequence occurs at the start of the line, not halfway through the line, so the odd and even fields can be distinguished.

The field sync. integrator consists of an up/down counter sampling the state of VCS every microsecond.It counts up when VCS is high, and down when VCS is low, but will not go below count zero. When a count of 37 is reached, a field sync. output pulse is provided (about 3/4 of a line after the start of the first field pulse). The integrating effect of this circuit permits noisy signals to be handled, which give rise to more edges in the VCS waveform.

When a field sync. pulse has been accepted by the acquisition timing chain, further field sync. pulses are ignored until at least 309 line periods have elapsed. This lockout mechanism gives a measure of protection against short-term disturbances which might otherwise upset field synchronisation and hence data capture. In the absence of a field sync. pulse the acquisition timing chain free-runs, maintaining the original phasing until a new valid field sync. pulse is available.

In the event of the signal being very noisy, the signal quality detector cuts off the field synchronising signal. This allows the timing chain to free-run, without being disturbed by noise output from the field sync integrator.

3.4 Display timing chain

The display line counter can be operated in a variety of modes, under control of the microcomputer and broadcasters. For the 312/313 line modes, interlaced and non-interlaced, the display line counter is reset every field to synchronise it to the acquisition line counter and hence the incoming broadcast. This is necessary for the display of subtitles and mixed picture with text. When non-interlaced 312/312 mode is chosen , the display counter resets itself from a decode and free runs independently of the broadcast.

The reset signal to the display line counter is normally taken from the composite sync. generator circuit . This in turn is initiated by decodes from the acquisition or display line counters as described above.

Although the selection of timing modes is normally under the control of the T0 and T1 bits in mode register R1 (see section 7), if the display page is a newsflash or subtitle (as indicated by the C5 or C6 bits set in the page memory) then 312/313 line interlaced mode will automatically be selected. This does not, however, apply to slaved timing mode.

When slaved timing mode is selected, the reset to the display line counter is taken from a second field sync. integrator instead of the composite sync. generator. This allows the display to be field synchronised to an external composite sync. signal ($\overline{SCS}$) applied to the $\overline{TCS}/\overline{SCS}$ pin input. The second field sync. integrator is much simpler than the one used in the acquisition timing chain, and detects a field sync. pulse merely by looking at the level on the $\overline{TCS}/\overline{SCS}$ pin at 17us after the (nominal) start of line. The composite sync. waveform supplied to EURO CCT in this mode must therefore be derived from a noise-free source (e.g. sync. countdown circuit).

Outputs from the display line counter go to the character generator circuit to control its timing, and also pass to the composite sync. generator.

3.5 Composite sync. generator

The object of the composite sync. generator is to provide the sequence of line sync., equalising and broad pulses shown in fig. 15 which are suitable for driving the display timebases via the $\overline{TCS}/\overline{SCS}$ pin. The signal is known as TCS (Text Composite Sync.).

The composite sync. generator supplies TCS waveforms appropriate to the selected timing mode, i.e. 312/313 lines interlaced, 312/313 or 312/312 lines non-interlaced. It is not used in slaved timing mode, when the $\overline{TCS}$ output buffer must be turned off (TCS ON = 0).

Decodes from the line rate timing are supplied to the composite sync. generator to derive the line sync.,equalising and broad pulses. It normally generates line sync. pulses until initiated by a signal from the acquisition or display line counters and then generates the sequence of equalising, broad and equalising pulses (each for two and a half line periods) until returning to line sync. pulses.

The composite sync. generator is thus an autonomous circuit, and does not rely on decodes from the line counters. Once initiated it will produce the field sync. sequence regardless of any other condition, thus avoiding some side effects which can occur with sync. disturbances in the first generation LSI decoder.

3.6 Signal quality detector

As mentioned previously, the signal quality detection function is not provided in VIP2 but is done digitally in EURO CCT.

When a very noisy video signal is applied to a teletext decoder, two undesirable effects can occur. Firstly the display phase locked loop may have difficulty in synchronising, and this gives rise to an unstable display of text on the screen. This may be so bad as to render it unusable for status display purposes. Secondly, the noisy video signal may be interpreted by the acquisition circuit as valid teletext data, thus writing rubbish into memory and corrupting previously received pages. These two problems can be solved by the use of a signal quality detector, which on detection of a bad or absent signal forces the display loop to free run and cuts off data to the acquisition circuit.

The method of signal quality detection used in EURO CCT is based on the number of pulses in the VCS signal per line period. Normally there is one pulse (line sync.) or two pulses (equalising or broad pulses) per line,but as the noise content of the signal increases extra spurious pulses are introduced into the VCS signal. They appear first near the field sync. period due to the a.g.c. action in the receiver and gradually increase until with noise-only input there are large numbers of pulses per line.

The basic criterion used to detect a bad line is that it contains three or more pulses. If the signal quality was previously good, more than 14 bad lines in a field cause the field to be declared bad. However if the signal quality was bad, less than 3 bad lines in a field are necessary to declare the field good. This gives hysteresis to prevent oscillation between good and bad signal quality on a marginally noisy signal.

Since the signal quality detector is required to operate when the display phase locked loop is free running, a further test is necessary. A line without any pulses on it could indicate no input and therefore bad signal quality, but an apparently blank line could be produced if if the oscillator free-runs too fast, as the line timing to the signal quality detector would have a period less than 64µs. Up to 31 blank lines without pulses are allowed per field before the field is declared bad. This allows a free running display oscillator running over 5% faster than the nominal 6MHz to be accomodated.

In order to ignore short term disturbances while giving a rapid response time the signal quality signal is obtained by integrating over 3 fields,i.e.three bad fields are required to go from good to bad signal quality, and three good fields change back from bad to good signal quality.

The switching points of the signal quality detector depend on the configuration and the nature of the noise. However the following values are a guide for a typical receiver situation with tuner, i.f. stages and synchronous demodulator where noise is introduced simply by attenuating the input signal. Signal to noise ratios of about 12.3dB cause a switch to bad signal quality, and when the signal to noise ratio improves to 13.4-14.2dB good signal quality is restored. These values are measured at the demodulator output.

When the bad signal quality condition is detected, this stops data flow through the acquisition circuit. It cuts off the output of the field sync integrator, and also normally removes the PL component from the SAND output, which is detected by VIP2 and causes its phase locked oscillator to free run. However if slaved timing mode is chosen (see 3.4 above) the PL output is always present, regardless of the state of the signal quality detector, as the phase locked loop is not attempting to lock to the incoming video signal.

3.7 Flash counter

The last part of the timing chain function consists of a divide by 32 counter for deriving the on/of signal for flashing characters. Driven from the 40ms (25Hz) frame rate output of the odd/even field flip-flop, it provides a 75% duty cycle signal with a period of 1.28 seconds.

3.8 Timing configurations

The normal operating configuration of EURO CCT in conjunction with VIP2 is shown in fig.16. A sync. signal to drive the timebase is output on the STTV pin on VIP2, and this can be selected by software control via EURO CCT. If the display is to be driven by the EURO CCT timing then the TCS ON mode bit is set to 1. This causes the output buffer on the $\overline{TCS}/\overline{SCS}$ pin to be activated, and the composite sync. waveform TCS appears on the STTV pin. Alternatively, when TCS ON is set to 0 the $\overline{TCS}/\overline{SCS}$ output buffer turns off and the line connecting the pin to VIP2 floats up to a higher than normal voltage level. This condition is sensed by VIP2, which then outputs the incoming video signal on the STTV pin so that the display is synchronised by the incoming broadcast.

An alternative method of connection using the slaved timing mode is shown in fig. 17. The composite sync. waveform controls the display timing, line synchronisation being performed in VIP2 and field synchronisation in EURO CCT. Note that the composite sync. waveform must be in line synchronism with the broadcast if teletext data is to be captured, although field sync. will still be taken care of independently by VCS. The high threshold voltage of the $\overline{TCS}/\overline{SCS}$ input pin allows a series flashover protection resistor to be employed, which is necessary if the sync. waveform source is some distance away.

4. Character Generator Function

This section describes the operation of the character generator and how it may be accessed to give displays in several languages. A block diagram of the character generator function is shown in fig. 18.

4.1. Interface Pins

The main outputs from the character generator are the R,G, and B pins. They provide the red, green and blue components of the text display.

An output for blanking the t.v. picture is provided, BLAN, which contains all the necessary signals for mix mode, boxing text or full screen blanking as appropriate.

Contrast reduction of the t.v. picture may be effected via the $\overline{COR}$ output pin. This allows not only mix mode displays with improved text legibility but also can give reduced contrast sub-titles with suitable interfacing circuits.

Finally, the Y pin outputs monochrome text display data, without background colours and ignoring the flash function. It is therefore suitable for driving a page printer.

All these pins have open drain outputs for maximum flexibility in the design of interface circuits. The delays of signals to these pins are carefully matched and resynchronised so that high quality displays may be achieved.

4.2. Display Format And Timing

A page of teletext as broadcast consists of 24 rows, each containing 40 characters. EURO CCT also provides an additional row for locally generated status displays, bringing the display format up to 40 characters by 25 rows.

Since the character display area must be kept away from the picture edges to allow for overscan, only 40µs out of the 51.7µs active line time is used for text display. In the vertical direction, 10 t.v. lines in each field are used per row of characters, making 250 lines in all out of 287 active lines. These characteristics are shown in fig. 19.

Each character rectangle thus occupies 1µs horizontally and 10 t.v. lines vertically. EURO CCT uses a character generator ROM with a matrix of 12 x 10 dots to cover the whole of this area, including spaces between characters, as shown in fig. 20. This high horizontal resolution allows much greater freedom in the design of character shapes, leading to better appearance and greater legibility. In general, vertical lines in characters are constructed using two adjacent dots, thus giving a 1/6µs wide output pulse. This requires the same video amplifier bandwidth as the first generation decoder.

The top line of the ROM matrix is normally blank, so that text in boxes or different coloured backgrounds is separated from the display above it. Accents above characters may require this line to be used, however. The bottom two lines are used for the 'tails' of descending characters like p and y. In the horizontal direction, characters are usually spaced by three dots, made up of two dots on the left and one dot on the right of the ROM matrix.

The 12Mb/s dot output rate is derived from the 6MHz clock F6, using both rising and falling edges. General timings of the outputs are, of course, synchronised to the display timing parts of the timing chain section. Both interlaced and non-interlaced displays can be selected, as explained in section 3. In the case of interlaced displays, the outputs are identical for odd and even fields.

4.3. Display Data Input

Data is supplied to the character generator function from the page memory via the memory interface circuit. There are two main groups of data required to generate a page of characters.

Firstly, there is the group of character codes which select the particular symbols required on the screen. These codes include alpha-numeric, graphics and control characters, which are accessed from the page memory in a similar manner to the first-generation LSI decoder. Several languages can now be dealt with; see 4.7 "Character Addressing Methods" below.

Secondly, a further group of data is required to indicate the status of the page, known as page attributes. This data is stored in a part of the memory which is not accessed directly for display. The page attributes used by the character generator function are the C5, C6, C7, C10, C12, C13 and C14 control bits from the page header transmission. In the first-generation LSI decoder these bits were dealt with directly in the chip logic. With EURO CCT, however, it is necessary to transfer the information via the page memory. This is because of the multipage facility, so that when a new page memory is selected for display the page attributes will change also.

Referring to fig. 18, the data input from the memory interface is applied to four circuits. The character address decoding circuit ensures that the correct part of the ROM is accessed for alphanumeric characters, taking into account the language selection bits C12, C13 and C14. Graphics characters (mosaics) are not stored in the ROM but are generated by the graphics decoder, which is followed by a latch to allow them to be held ('hold graphics' facility). Display control functions are dealt with by the control character decoder. This has the same 'level 1' capability as the first-generation LSI decoder, but with the addition of 'alphanumerics black' (0/0) and 'graphics black' (1/0) control characters, thus allowing black text to be generated on a coloured background. Finally, decodes from the display timing cause the state of the page attributes to be updated once per field in the page attribute latches.

The page attributes are dealt with as follows. Newsflash and subtitle control bits C5 and C6 are treated together to give an output if either is set. This output selects the appropriate display control register, R5 or R6, and is also used in the timing chain (see section 3). The suppress header bit C7 inhibits the display of row 0 when set to a 1, although the header data is still written to the page memory. Similarly, if the inhibit display bit C10 is set to 1, rows 0 to 23 inclusive are not displayed. It should be noted that these row numbers refer to storage in the memory, not necessarily row numbers on the screen. The status row, row 24, is always displayed whether it is at the top or bottom of the screen. Language selection bits C12, C13 and C14 are used for character address decoding as described in 4.7 below. Finally, each page has a 'page being looked for' attribute PBLF, which is used in the acquisition function (see section 5).

4.4. ROM And Associated Circuits

The ROM in EURO CCT contains 128 characters, each stored as a matrix of 12 dots horizontally and 10 dots vertically. The 128 characters are selected by the character address decoding, and the 10 lines by the ROM line address decoding. Since the ROM is accessed once per microsecond, twelve outputs are provided from the ROM matrix, corresponding to the twelve dots in a line of a character.

A multiplexer at the ROM outputs selects either the ROM or the graphics decoder depending on the state of the alphanumerics/graphics control function. The twelve outputs are loaded every microsecond into two 6-bit shift registers which are clocked with opposite phases of the 6MHz clock derived from F6. In this way one shift register deals with odd-numbered dots in a character, and the other with even-numbered dots.

The two 6MHz dot streams are multiplexed together by both states of the 6MHz clock in the combined multiplex logic and output buffers, thus giving a 12MHz dot rate. Inputs to the multiplex logic determine the required foreground and background colours, flashing, etc. An enable pulse from the memory interface is also supplied to give a cursor display. The cursor follows the active row and column registers R9 and R10 regardless of the selected active chapter. It inverts foreground and background colours, e.g. a red character on a black background becomes a back character on a red background rectangle.

The output buffers, R, G and B supply red, green and blue dot information respectively. The Y output is active for the character foreground only, regardless of colours, and does not contain the flashing function. Blanking signals for the t.v. picture are supplied through the BLAN pin, being combined dot, box and full screen blanking.

4.5. Display Address Counters

A 64µs rate signal from the timing chain clocks the lines per row counter. This counter normally divides by ten, and its outputs are used to select the appropriate line of twelve dots in the ROM. Double height characters may be present, however, and in this case the double height control rearranges the addresses to the ROM so that each line of dots is accessed twice, the counter dividing by 20 instead.

A decode from the lines per row counter clocks the divide by 25 row counter, which is responsible for addressing the memory for display. This counter can be controlled to give the status row (row 24) display at the top or bottom of the screen, and also to give user-selected double height characters. Decodes from this counter are sent to the double beight control so that double height control characters are ignored in row 23 and row 24. They are also ignored in row 11 when user-selected double height is activated. Outputs from this counter are also used in the display control circuits. If a double height control character is present, the row address is maintained for 20 lines instead of 10 lines. This is the purpose of the latch at the row counter output.

In the event of both user-selected and broadcast double height being present, quadruple height characters will be obtained.

When user-selected double height is activated, either rows 0 to 11 or 12 to 23 are displayed with double height characters according to the state of the top/bottom control function. It should be noted that the status row, row 24, is always displayed in single height characters only, whether it is at the top or bottom of the screen. If a double height status message is required (e.g. program name in television mode) then the first seven characters in row 0 may be used, as these respond to the double height command.

4.6. Display Control Circuits

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The display control circuits take information from the display control and mode registers, page attribute latches, control character decoder and row counter. They use this information to control the display via the output multiplex logic.

Basically there are four control functions: t.v. picture, text, background and contrast reduction. Each of these functions can be on or off under software control. They are stored in the display control registers R5 and R6, one of which is automatically selected for a normal page or a newsflash/subtitle. This allows the control software to predetermine which functions are required for each type of page, without having to know when the displayed page changes its type.

Often the kind of display required will change depending on the 'start box' and 'end box' control characters. Independent control of the display functions is therefore provided inside and outside the boxing function.

The boxing function may be enabled for certain areas of the screen only, if required. For example, a status display on row 24 may be required, boxed in a t.v. picture. In this case, boxing would only be allowed on row 24, and text only in boxes. This stops any newsflash (received in row 20, say) being displayed as well as the status message.

The t.v. picture function operates via the BLAN pin, i.e. when t.v. picture is on there is no blanking. This function operates within the text display area according to the boxing function with PON IN and PON OUT. Outside the text display area the state of PON OUT is used to determine whether the t.v. picture is present or not. As well as t.v. picture being off, the BLAN pin is activated to provide blanking whenever text is on and background is on, or when text is on and a foreground colour is being output. This allows boxed and superimposed text displays to be generated.

The text function enables the R, G, B and Y text outputs according to the boxing function with TEXT IN and TEXT OUT. It operates during the text display area only.

The background function enables the display of background colours on the R, G, B outputs when text is on, as well as foreground colours. It operates according to the boxing function with BKGND IN and BKGND OUT. If the background function is off only foreground colours will be displayed. The area normally occupied by the background colour will then be either black or t.v. picture depending on the state of the t.v. picture function. The background function overrides the t.v. picture function, so that if both are on at the same time no t.v. picture will be obtained, even if the background colour is currently black.

The contrast reduction function operates via the $\overline{\text{COR}}$ pin, which goes to the low state whenever contrast reduction is required. This function operates according to the boxing function with COR IN and COR OUT during the text display area. Outside the text display area the state of COR OUT is used. The $\overline{\text{COR}}$ output comes directly from the display control circuits, as it is a static or character rate signal without dot rate information. It is, however, carefully resynchronised to be in step with the R, G, B, BLAN and Y outputs. The output may be connected to a high-speed contrast control point in the t.v. receiver video circuitry to allow subtitles in reduced contrast boxes. Alternatively it may be used as a static signal for mix mode, like the $\overline{\text{Superimpose}}$ output of the first-generation LSI decoder.

When characters are concealed by the appropriate control character, they are displayed as if they were spaces until the conceal/reveal control bit is set to 1. Flashing characters are effectively replaced by spaces during the 'off' time of the flash (25% of the 1.28 second flash cycle time).

Inversion of a character for the cursor acts after these space-forcing functions. For example, a red character on a green background is displayed as a green space when concealed; moving the cursor to this position results in a red square.

The same rules apply to black as any other colour for either foreground or background. When enable signals are activated for either foreground (text on) or background (bkgnd on), the t.v. picture will be blanked even if 'picture on' is requested and the colour is black.

4.7. Character Addressing Methods

EURO CCT has the capability of displaying text in different languages. There are basically two methods of accessing the ROM, depending on the facilities required.

The first method is used when only one language is required per page, and is the normal way of operating for 'level 1' teletext. A seven bit code table is in use, having 32 control characters and 96 display characters, and bit 8 is always 0. The 96 characters form a 'national option' character set, and any one of three possibilities is automatically selected by the C12, C13 and C14 control bits contained in the page header transmission.

The character set selection codes are mask programmable, as are the dot matrix patterns. However, the first version of EURO CCT contains English, German and Swedish character sets as shown in fig. 21. The character sets differ only in the 13 national option characters indicated, and are selected by the following codes:

C12	C13	C14	
0	0	0	English
0	0	1	German
0	1	0	Swedish

Any other combination of C12, C13 and C14 selects the English character set. It should be noted that the state of these control bits is taken from the stored page in memory, so that when a different page is selected for display the language can change immediately.

This 'seven-bit' method of accessing the ROM gives multiple language operation without the need for any intervention by the control microcomputer.

The seven-bit method does have disadvantages, however. First of all, it is not possible to mix languages on a single page. More seriously, locally-generated status messages will be in a given language which should not change even though the language of the broadcast page may vary. The 'eight-bit' addressing method provides a solution to this problem.

When bit 8 is set to 1, a second version of the code table is accessed, as shown in fig. 22. This consists of the German character set, repeated in columns 10 to 15. Columns 8 and 9 contain the English and Swedish national option characters, respectively, together with some special symbols. None of the characters in fig. 22 are affected by the language control bits C12, C13 and C14; they always remain the same. All of the 128 available character shapes in EURO CCT may be addressed unambiguously with bit 8 set to 1.

Thus the variability of any character may be defined: if bit 8 is 0 it will follow the transmitted language, if bit 8 is 1 it will remain fixed. A combination of both methods will normally be used to give automatic language selection for the broadcast page with status messages remaining fixed.

It is also possible to mix languages on the broadcast page. Additional information transmitted in ghost rows 26 (see section 5) allows characters to be altered from the default 'level 1' page. This information can be received by EURO CCT, and then processed by the control microcomputer which overwrites the code in the page memory using the 'eight bit' method. Although the 128 character set in EURO CCT does not allow for all the defined ghost row codes, it is certainly possible to have the three languages available on the same page.

Another use of the ghost row processing technique is to provide status and control messages which are in the same language but are invisible to existing 'level 1' decoders. This feature may become very important for the more sophisticated type of decoder to give better user controls, pseudo-interaction etc., especially on cable t.v. systems.

The same kind of technique may be used by the microcomputer to process escape sequences in wired systems to give a multiple language display capability.

Dot matrix patterns for the first version of EURO CCT are shown in fig. 23.

Mosaic graphics are available when in graphics mode by accessing columns 2,3,6,7,10,11,14 or 15 (same symbols regardless of bit 8). However, 'blast through' alphanumerics characters can only be accessed in columns 4 and 5 when in graphics mode. Columns 8,9,12 and 13 all produce a space in graphics mode.

All control characters must, of course, be accessed with bit 8 = 0 as in fig. 21. EURO CCT has provision for all the normal control functions of level 1 teletext (alphanumerics/graphics, colours, flash, conceal, boxing, double height, background colours, separated and contiguous graphics, hold graphics), plus black foreground colour as mentioned earlier.

4.8. Interface Circuits

All the output pins of the character generator have the open drain configuration, and many interfacing arrangements are possible. Some general points should, however, be taken into consideration when designing interfaces.

Although the output pins will accept relatively high voltages, the technology imposes a limit on current sinking capability (see specification). This current charges the load capacitance on the pin when the output switches off, and so the rise time may be relatively slow. It is recommended that the output amplitude be kept to the minimum required for the application to minimise the effect. A typical circuit will include a pull-up resistor supplying current to the pin from a relatively high voltage (e.g. 5V or 12V), but will also have a diode clamp limiting the maximum voltage on the pin to e.g. 1 or 2V. The clamp voltage may be variable to give a text contrast control, as shown in the application circuit of fig. 5.

The fall time of an output is largely determined by the load capacitance, as the output transistor is switched on. In view of the high speed of the text outputs (e.g. the R,G,B and Y pins may contain 83ns wide pulses) the load capacitance should be kept to a minimum. The video circuits into which they feed must therefore be as close as possible, otherwise the text outputs must be suitably buffered. As the video circuits are often some distance away from the text decoder, buffering the outputs is usually carried out. This is also desirable for reasons of flashover protection.

If the text decoder is incorporated into the main receiver circuit board it may be possible to arrange the board layout so that interfacing components are greatly reduced, provided care is taken with load capacitance and flashover protection.

The R,G, and B outputs are active high for red, green and blue text signals respectively. An active high signal to blank the t.v. picture comes from the BLAN pin, containing full screen, box and dot blanking. No further gating of this signal is necessary. An active high monochrome text signal without background colours or the flash function is provided on the Y pin; this is suitable for driving a printer. Finally the $\overline{COR}$ pin is active low whenever contrast reduction of the picture is required.

All these signals are resynchronised internally from the F6 input.

An output interface circuit suitable for use with the TDA3560 colour decoder is shown in fig. 24. This is similar to that used with the first generation LSI decoder, but also contains provision for fast contrast reduction to give improved subtitle displays.

An output interface suitable for driving an external monitor for a text-only aplication is shown in fig. 25. This gives a 1 Volt signal into a 75 ohm load.

Interface circuits for an add-on adaptor are shown in fig. 13.

5. Data Acquisition Function

This section describes the data acquisition function and how it may be used in various ways to cover a number of applications.

5.1. Interface Pins

Three pins on EURO CCT connect to the data acquisition function.

Serial data from the SAA5230 (VIP2) Video Input Processor at 6.9375Mbits/sec is applied to the TTD (Teletext Data) pin via an external coupling capacitor. The TTD pin is provided with an internal clamping transistor, which is turned on from time 4µs to 8µs every line period. During this time the SAA5230 Video Input Processor holds its output at the 0 logic level, and d.c. restoration at the EURO CCT input is obtained. The capacitor value must be large enough to ensure that the data level does not sag too much over the line period as a result of leakage current.

The 6.9375MHz clock TTC is used to shift the teletext data into EURO CCT. The rising edges of the clock are nominally at the centre of the valid data period. As the SAA5230 Video Input processor provides a continuous clock, a simpler interface arrangement is possible. The clock is applied directly to the TTC pin on EURO CCT, and there is on-chip capacitive coupling to change the d.c. level. A fed-back inverting buffer arrangement ensures that the clock is sliced internally so as to produce a duty cycle close to 50%.

Both the TTD and TTC signals from the SAA5230 have reduced edge speeds and amplitude to minimise the risk of interference with other parts of the t.v. receiver.

An output from the acquisition circuit is applied to the HOK pin. This is a flag indicating for each line whether a valid teletext signal has been received or not. The criterion for the data line to be valid is that all eight bits of the framing code must be correct, and the first two Hamming bytes (i.e. magazine and row address) must have no uncorrectable multiple errors. The signal name HOK derives from 'Hamming bytes OK'. When the data line is valid the HOK signal will go high between 18 and 23µs into the line, and remain high until 7µs into the next line. If the data line is invalid the HOK signal remains low. The HOK signal can be sent to an external microcomputer or logic to provide drive waveforms for an echo equaliser circuit if required. Decoders without an echo equaliser have no connection to the HOK pin.

5.2. Data Acquisition Principles

The principles used by the teletext transmission for the acquisition of data will be summarised to aid understanding of the acquisition section.

Every teletext data line has two Hamming coded bytes which contain the magazine and row address. The magazine number (1 to 8) is the 'page hundreds' digit, and the row number allows three types of data lines to be distinguished.

Data lines with row address 0 are page headers. These contain 8 further Hamming coded bytes, which give the page number (tens and units), page sub-code (formerly time code) of four digits, and a number of control bits. In the remaining 32 characters for display are the service name, date and page number, with the last 8 characters specially reserved for time.

Rows 1 to 23 are normal rows containing data for the display page.

Rows 24 to 31 are ghost rows, so called because they are ignored by the first-generation decoders. Certain of these have now been allocated defined functions, and they can be received by EURO CCT if it is switched into ghost row mode. They allow more sophisticated decoder facilities, as explained later.

The rows received by EURO CCT are summarised in fig. 26, together with their structure and functions.

Acquisition of a page depends on the sequence of data in relation to a page header. When the page header for a requested page is received, a flip-flop is set (known as the CPHR flip-flop: correct page header received). This permits normal rows of the correct magazine number to be stored, until the process is terminated by the arrival of another page header which resets the flip-flop.

Special treatment is given to the storage of the page header. If the page header is "valid" (i.e. has the correct magazine number in parallel magazine mode), the last 8 characters are stored regardless of the requested page. In this way, the clock time at the top right of the screen is kept updated. Similarly, when a page is being searched for (but has not yet been received) the remaining 24 display characters of a valid page header are also stored, producing a 'rolling header' effect with rotating page numbers. This status is stored by a P8LF (page being looked for) flip-flop, which is set after a page request and is reset on the first reception of the correct page header.

Most ghost rows contain data related to a particular page, and are dealt with in a similar manner to normal rows. It should be noted that some ghost rows have sequence numbers (shown by S in fig. 26), allowing several data lines of the same row number to be transmitted.

Some ghost rows have special treatment, however. The magazine related version of row 28 is stored for the correct magazine regardless of requested page number. Also row 30 is always stored, whatever the magazine or page number. More details are given in 5.15 below.

Complications to these basic techniques include serial and parallel magazine modes, where the data is considered to be either from one database or eight entirely separate transmissions, possibly interlaced. Also the other page header control bits need to be dealt with. The effect of these details will be mentioned in the relevant sections.

Another factor to be taken into account is page clearing. This is carried out in field flyback mode on the first reception of a page header, recognised by both the CPHR and PBLF flip-flops mentioned earlier being set. The transmission facilitates this action by allowing one field period between the first reception of a page header and normal rows for that page. Page related ghost rows should also be cleared in the same way. In full channel mode the 'advance warning' restriction is unworkable and so other methods must be used; see 5.16.

5.3. Requesting A Page

There are seven digits to identify a page: magazine (page hundreds), page tens, page units, hours tens, hours units, minutes tens and minutes units. The last four digits are the sub-code, their names derived from the earlier application as time coded page digits. These are still used for time selection with the 'alarm page' provided by the broadcasters, but in general they are versions of a page and have no connection with clock time.

In the first generation LSI decoder there were two methods of requesting a page - normal and timed page. For normal page requests three digits were used, and the sub-codes were ignored. In timed page mode, all seven digits had to be correct before a page was received.

With EURO CCT a much more flexible method is used. Each digit has associated with it a flag which can be set to indicate whether the digit should be ignored or not for page comparison. Any combination of flag states may be used. If a 'don't care' flag setting is denoted by X, the following examples show the operation of the method.

523XXXX	requests page 523 (normal)
5231400	requests page 523, sub-code 14.00 ("timed page")
5X3XXXX	will receive pages 503, 513, 523, 533, 543 etc., as transmitted
XXX1400	will receive any page with sub-code 14.00
2XXXXXX	will receive all pages in magazine 2
253X1XX	will receive page 523 provided the `hours units' sub-code is 1.

This arrangement, in conjunction with EURO CCT's priority system for multipage acquisition, allows pages to be acquired when the full numbering allocation and transmission sequence is not precisely known in advance.

The requested page numbers, together with do/don't care flags, are loaded by the control microcomputer via the IIC bus into on-chip RAM in the acquisition section of EURO CCT. Also included is an overriding 'hold' facility, which stops the updating of the page if required. The format of the data sent to the on-chip RAM is shown in fig. 27.

It is also possible with EURO CCT to request pages in the full hexadecimal range, not just BCD digits. This is necessary for the acquisition of higher levels of teletext and telesoftware. Each digit has a varying number of bits, as can be seen from fig. 27; the highest page number possible being (hex) 7FF3F7F. Note that magazine 0 (hex) is actually labelled 8 for the user display. Using the full hexadecimal range, there are 4,194,304 combinations of page and sub-code numbers.

5.4. Multipage Acquisition

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In order to receive a page, the data in the page request RAM must be compared with the current incoming page header, and the CPHR (correct page header received) flip-flop set if the two match. This will then allow normal rows to be written into the external page memory.

The EURO CCT acquisition section is capable of searching for four pages simultaneously, and in general the system operates as if there were four entirely separate acquisition circuits. Each circuit has its own page request RAM, comparator, CPHR (correct page header received) flip-flop, PBLF (page being looked for) flip-flop and clear control circuits.

To request a page, the acquisition circuit required (one of four) is selected in register R2 using bits D4 and D5. These bits correspond to memory address lines A10 and A11, i.e. each acquisition circuit is associated with a particular memory. When ghost row mode is selected the most significant memory address A12 is used to distinguish normal and ghost row information for storage.

If ghost row mode is not used, however, eight pages may be stored. The 'bank select' bit in register R2 (D6) may then be set to give the A12 address state required. It should be noted that 'bank select' applies to all four acquisition circuits simultaneously; the choice is made between acquiring data into memory addresses 0,1,2 and 3 or 4,5,6 and 7. Once the 'bank select' mode bit is altered, previously stored pages will be retained but will no longer be updated.

When writing to register R2, the 'start column' is also defined in bits D0, D1 and D2. The column relates to the information written to register R3, as shown in fig. 27. Often the start column will be set to 0, as this defines the 'magazine' digit which is normally the first to be written into EURO CCT. The register R2 address automatically increments to register R3, so the next IIC byte will be magazine number and subsequent bytes page tens, page units etc. Fig. 28 shows the organisation of register R2, together with an example of a page request IIC bus sequence (more information in section 7).

One point to be borne in mind when requesting pages is that reception should be inhibited when page request numbers are being written, otherwise unintended pages may be captured. For example if the previous page request was 100 and this is being changed to 234, it would be possible to capture page 200 if it arrived just after the page request digit 2 had been entered. There are two methods of dealing with this situation.

Firstly, if the new page is being requested as a continuous IIC transmission, EURO CCT performs the temporary hold function automatically. As soon as register R3 is written to, a temporary hold function is activated until the IIC transmission has ended. This transmission will all be related to a page request for that acquisition circuit as register address R3 does not auto-increment. Note that the temporary hold function only applies to the acquisition circuit being written to; the flow of data through the other three acquisition circuits is not interrupted.

The second method is used when the control software sends page request digits to EURO CCT one at a time, with breaks in the IIC transmission between digits. In this case the software designer is responsible for controlling the hold function provided, to give the required action. When the IIC transmission for page digits ends, EURO CCT assumes this means a page request. This could be one, three, seven or another number of digits - EURO CCT does not know whether to expect any more. The control software should set the hold function (by writing register R3 column 0 bit D3 to 0) as the first action on page request, and return to reset the hold function when all the desired page request functions have been set up.

The main difference between the multipage acquisition circuit of EURO CCT and four separate single-page decoders lies in the treatment of common page requests. Each page coming into EURO CCT can only be written to one memory at a time. If a page being received is requested by more than one acquisition circuit, a priority arrangement ensures that it is written only to the lowest valid memory address (equivalent to the lowest numbered acquisition circuit).

For example, suppose that page 123 is requested in acquisition circuit 0, page 1X3 in acquisition circuit 1, and 1XX in acquisition circuit 2. As the highest priority, page 123 will be written into memory 0. All other pages conforming to 1X3 (i.e. 103, 113, 133 etc., but NOT 123) will go to memory 1 as this is the second priority. All other pages in magazine 1 go to memory 2. If the order were to be reversed, with 1X3 in acquisition circuit 0 and 123 in acquisition circuit 1, memory 1 would never be written to as its page request is common to a higher priority acquisition circuit.

Using appropriate control software, the priority arrangement can be exploited to give more sophisticated acquisition techniques. For example, suppose a rotating page is being transmitted on page 350, with sub-codes being used to distinguish the variants. The operator need not know how many rotating pages there are, but wishes to capture and read them in the correct sequence. Initially the software selects page 3500001 in acquisition circuit 0, 3500002 in circuit 1, 3500003 in circuit 2, and 350000X in circuit 3. This captures the first three sub-pages in the correct order, and the software can examine the contents of memory 3 to determine whether there are more rotating pages. If so, it can take steps to reallocate page requests in memory 0 when the operator has finished looking at the first page in memory 0. Memory 3 can thus be used to search for further pages without interfering with the reception and updating of the existing pages.

Another technique would be to request page XXXXXXX in memory 3. This then receives any page apart from the others requested, and the control software can read the number of the currently transmitted page. In conjunction with some knowledge of the transmission sequence the decoder could be made to optimise the time to request a page from several in a list. For example, if pages 101, 102, 103, 119, 127, 134, 136 and 188 were required, and the current page was 129, the control software could request page 134 first as this would be likely to arrive before the others.

5.5. Stored Data

Each page captured by the acquisition circuit contains not only the characters which make up the display, but also control and address information. This information is stored in row 25 of the memory, which is not displayed but may be read via the IIC bus.

The format of this data is shown in fig. 29. It occupies the first 10 bytes in the row, leaving the remaining 14 for use by the microcomputer if required as general purpose RAM. All the page addressing information is stored in the memory after Hamming check, and relates to the page actually captured into that memory. Each byte contains four bits of information, and has associated with it a Hamming error flag. This flag is set to 1 if there has been an uncorrectable multiple error. If there has been only a single bit error this is corrected by the Hamming circuit before storage in memory and the Hamming error flag is not set.

The 'magazine' address data does not have an associated Hamming error flag. This is because the original byte in the transmission shares one bit with the row address, and if there were a multiple error here the data would be rejected, as it is uncertain whether the data line is a page header. As far as the other address bytes are concerned, it is possible to have the Hamming error flags set as a result of 'don't care' settings in the page request RAM. For example, a Hamming error in the 'minutes units' byte would not prevent the capture of a normal (non-sub-coded) page. If, however, there is a Hamming error in an address for comparison, the page will not be received on that occasion. Old address data stored on the previous reception of the page will be retained.

The Hamming error flags may be used by the control software to provide different actions when the data is not reliable.

As well as addressing information row 25 also contains the control bits from the page header (C4-C14). The treatment of these varies according to their function, as listed below.

C4, erase page, is dealt with by the acquisition hardware on reception of the page, in field flyback mode only. Rows 1-23 are cleared to 'space', and also rows 0-21 of the associated ghost row memory in ghost row mode. This clears all the page related data. Memory write cycles outside the data entry period are used for this function, see 5.13. The state of C4 in row 25 is representative of the last page capture. As this function is used transiently by the broadcasters, it will normally go low again on the next transmission of the page.

C5 and C6 are the newsflash and subtitle control bits respectively. They are stored in row 25, and are then used by the display and timing functions to give automatic display control, as explained in sections 3 and 4 above.

C7 is the suppress header control bit. After storage in row 25, it is used to disable the display of row 0 as explained in section 4.

C8 is the update function. This bit may be set by the broadcasters to draw the viewer's attention to a page when the information on it has changed. In the first-generation LSI decoders it was brought into use by the 'display cancel' function. No action is taken by the EURO CCT hardware when this bit is set. It is up to the control software to decide what action to take (if any) on the setting of this bit, by examining row 25. Actions might include generation of a status message, immediate display of a newsflash, etc.

C9 is the interrupted sequence indicator. This bit is set by the broadcasters to indicate a page transmitted out of the normal sequence, so that discontinuities in rolling page numbers can be avoided. The appropriate action is taken by the EURO CCT hardware before storage of rolling headers.

C10 is the inhibit display control bit. After storage in row 25, it is used by the display section to stop the page being displayed as explained in section 4. The page is still written into memory, however, and may be read via the IIC bus.

C11 is the magazine serial control bit. It indicates whether the broadcast is to be regarded as a complete unit with all page numbers possible (serial), or whether each magazine should be treated completely independently of the others (parallel). This bit is dealt with by the acquisition section hardware. Note that this bit should be set to the same state on all data lines of a transmission, otherwise the decoder will be confused as to the exact actions required.

C12, C13 and C14 are the language control bits. They are written into row 25 by the acquisition circuit, and are then used by the display circuit to change languages automatically as explained in section 4.

In addition to the control bits and addresses, two further functions are written into row 25 by the acquisition hardware to facilitate decoder control. These are the PBLF and $\overline{\text{FOUND}}$ functions.

The PBLF function is written to row 25, column 9, bit D5. It represents the state of the PBLF (page being looked for) flip-flop in the corresponding acquisition circuit. This signal is used by the EURO CCT hardware, and may also be read by the control software if required.

It will be recalled that the PBLF flip-flop is set on a page request, and is reset on first reception of the page. During this time the decoder indicates to the user that page search is in progress. It does this in two ways: firstly by inserting an 'alpha green' control character at the start of the displayed header row, and secondly by allowing all valid page headers to be received. This gives the familiar green rolling header of the first-generation LSI decoders. However, EURO CCT is a multipage decoder, with four PBLF flip-flops; also the memory being displayed can be changed by the control software at any time. The state of PBLF is therefore taken from row 25 of the current display chapter for the rolling header functions.

One small complication arises in the use of the PBLF bit, however. Although it is written fairly quickly on request and arrival of the page, limitations of RAM accessing mean that it can only be sensed by the hardware once per field. This would be a problem if, for example, the display chapter were changed from a memory with PBLF high to another with PBLF low and a page already received. The rolling header could continue for some time after the display chapter was changed, thus over-writing the previous correctly-received header with irrelevant information, in particular the wrong page number. This difficulty is overcome by the use of a flip-flop for the rolling header control which is instantly reset by any IIC write to register R4 (display chapter), as well as reception of a page. It is not set again until two fields have elapsed with the PBLF bit being consistently set to 1. On changing display chapter it is therefore possible that there will be a short interruption to rolling headers when they are still required, but correctly received headers will not be overwritten.

A further factor should be borne in mind when writing control software. At power-on, all memory locations are cleared to 'space', which sets a 1 into bit D5. This is the bit used for PBLF in row 25 column 9. The state of this bit will revert to 0 in chapter 0 on completion of memory clearing, as a different memory cycle is addressed for this purpose by the 'active' acquisition circuit (number 0 after power-on). However, the PBLF bits in all the other memory chapters will remain at 1. They will revert to 0 as soon as the appropriate acquisition circuits in register R2 are addressed.

Normally this does not matter, but if a different display chapter is selected after power-on before that chapter has been addressed for acquisition in register R2, green rolling headers will be displayed even although there has not been a page request. It is expected that the control software would not usually allow this possibility. However, if a multipage decoder is envisaged where this mode of operation could occur, it is suggested that the control software should cycle round the available acquisition circuit/memory chapters in register R2 after power-on. This will reset all the PBLF bits in row 25 to zero, stopping the display of green rolling headers. It is not necessary to write page requests into register R3 for this, addressing in register R2 is sufficient.

The PBLF bit is reset automatically on receipt of a page, independently of the active address in register R2.

The PBLF bit is set and reset by the EURO CCT hardware, as noted earlier. This is not the case for the $\overline{\text{FOUND}}$ bit, (row 25 column 8 bit D4), which is only reset by the hardware. Three states need to be determined in the acquisition control. Firstly, there is the normal state, when a page has been received, is being displayed, and all relevant control functions have been dealt with by the microcomputer. This is indicated by PBLF at 0 and $\overline{\text{FOUND}}$ at 1. Secondly, after a page has been requested and search is in progress, PBLF is set to 1 and $\overline{\text{FOUND}}$ is at 1. Finally when the page has been received but the microcomputer has not yet observed that fact, this is indicated by PBLF at 0 and $\overline{\text{FOUND}}$ at 0.

When the microcomputer has dealt with any actions necessary on receipt of the page, it should write a 1 to the $\overline{\text{FOUND}}$ bit. This then acts as a flag to the control software that action has been taken and it need not process that page again. Every time the page is received the $\overline{\text{FOUND}}$ bit will be reset to 0, indicating to the microcomputer that action may be required (e.g. page may be updated or different ghost rows transmitted). If no special action is taken by the control software on receipt of a page there is no need for the processor to write to the $\overline{\text{FOUND}}$ bit, which will then stay at 0 after the first reception of a page following power-on.

The actions of the PBLF and $\overline{\text{FOUND}}$ bits are shown in fig. 30.

5.6. Magazine Of Display Chapter

It is necessary to know the magazine number requested in the display chapter for various reasons. In parallel magazine mode, indicated by control bit C11=0, rolling headers must only be taken from the correct magazine. The clock time, too, must come from the correct magazine, as this may not be synchronised to other magazine transmissions coming from different sources. In ghost row mode, only the magazine related ghost row 28 appropriate to the display chapter is stored (see 5.15).

The magazine requested for each memory chapter is of course stored in on-chip RAM; however, it is impossible to read this data and get it to the control part of the acquisition section for reasons of chip architecture. EURO CCT therefore incorporates a circuit to store the latest magazine request in the display chapter.

After power has been applied to EURO CCT, before any page requests have been made, the circuit resets to magazine 1. This means that broadcast time will be received from magazine 1, and any 'time' control which may be provided for t.v. mode operation will still work before any teletext page requests are made. In serial magazine mode, of course, time is received from all magazines.

When a magazine number is written to register R3 for the memory chapter which is currently being displayed (address in register R4), the circuit is updated with that magazine number. This ensures that the correct rolling header is displayed in parallel magazine mode. Note that if a request is made for a different magazine number in another memory chapter (not the display chapter), and then that memory chapter is moved to the display before the page has been received, the wrong rolling headers will be displayed. The correct header will, however, be captured and the rolling will stop when the page has been received. This may be slightly confusing to the operator but does not stop the correct reception of a page. In serial magazine mode there is no difficulty, of course.

It should be noted that the circuit still takes account of the requested magazine number in register R3 even if 'don't care magazine' is also requested. Only one magazine is displayed for rolling headers to avoid a meaningless jumble of information, even though for actual capture of the full page any magazine is sufficient.

5.7. Serial To Parallel Conversion

A block diagram of the acquisition section is shown in fig. 31.

Inputs from the SAA5230 Video Input Processor are applied to the TTD and TTC pins; these are serial teletext data and clock respectively. The signals are buffered as described in 5.1 above, and applied to the serial to parallel converter. This circuit operates only when the 'enable acquisition' signal from the timing section is valid, during lines 6 to 22 inclusive in field flyback mode ($\overline{DEW}$/FULL FIELD = 0), or all lines in full field mode ($\overline{DEW}$/FULL FIELD = 1).

The serial to parallel converter operates by searching for the framing code (11100100) in the serial data stream. This must occur in a 3µs wide time window starting at 12µs into the line in order to be recognised. It is necessary for this criterion to be valid to stop the acquisition circuit misinterpreting other data as teletext, for example test insertion signals. The 3µs wide window takes into account the tolerance in the position of the broadcast data on the line (1.4µs), delay through the VIP circuit, VIP output and EURO CCT input buffer delays, and the locking accuracy of the VIP-EURO CCT phase locked loop, which determines where EURO CCT thinks the line sync edges of the video signal are.

Once the framing code has been recognised (all 8 bits correct) the serial data stream at 6.9375Mbits/sec is converted into 8 bit wide parallel data bytes, one byte being transferred every 1.15µs. The data acquisition logic up to this point has been of the static type, operating asynchronously. For reasons of circuit complexity and size, however, it is desirable to perform the majority of the function in dynamic synchronous logic, operating at a system clock speed of 1.0MHz. A resynchronising function therefore follows serial to parallel conversion, so that all data bytes are related to 1MHz system clock edges. Since the byte rate is slower than 1Mbytes/sec, about every 7 bytes the system clock "catches up" with the incoming data, and the same data is output twice on consecutive clock cycles. The resynchronising logic incorporates a signal to indicate whether the data for that clock cycle should be taken account of or not, and this is used to enable the byte counter circuit.

With the exception of the on-chip RAM section, all other parts of the acquisition function are performed synchronously at 1MHz using dynamic logic.

5.8. Data Checking And Delays

The address parts of the teletext transmission are Hamming encoded, whereas the data parts are protected by parity. Information from the serial to parallel conversion circuit is checked appropriately in the Hamming and parity check circuit. In the case of Hamming coded data, the eight bits in the incoming byte reduce to four information bits, but single bit errors can be corrected and two bit errors detected. A Hamming error flag bit is added to the four information bits, the remaining three bits of the outgoing data being set to 0. For parity checked data, a parity error is recorded as a separate signal (not shown in fig. 31) which stops that byte being written into memory. The most significant bit of the outgoing data is set to 0.

When 8 bit mode is selected, however, (register R1 bit D6 set to 1) parity checking is disabled and all eight bits are always written to memory. Hamming checking in 8 bit mode is carried out as normal.

The Hamming and parity checked data byte streams are combined by the multiplexer, which selects the correct type of data at the appropriate time. This data is passed on to other parts of the acquisition function.

The first two bytes (comprising the magazine and row address) are checked for Hamming errors by the HOK logic. If they are error-free a pulse is output on the HOK pin, as explained in 5.1 above.

As will be seen below, the acquisition function will accept a page only after all address bytes in a page header have been checked. These bytes require to be written to memory (see 5.5), and there is also a time delay before the page is recognised as correct. It is therefore necessary to delay the data before it is applied to the memory interface. This is performed by shift registers operating at 1MHz in the delay circuit. Overall delay, from data being applied to the TTD pin until the byte is written to memory via the memory interface, is 19-20.5µs.

5.9. Byte Counter

It is necessary to keep track of the data as it comes in, so that each byte can be allocated the correct function. This operation is performed by the byte counter, which is reset at the start of every line period and counts enable pulses from the serial to parallel conversion and resynchronisation circuit. Decodes from the byte counter perform various functions in the acquisition section. One delayed decode is used for clocking the column counter, which allocates column addresses to the memory interface in synchronism with the delayed data being applied to the memory interface. The column counting sequence is arranged to suit the various memory cycle functions, as explained in section 6 below.

Another delayed decode is responsible for enabling the write control at the appropriate times to write data into memory. Note that these delayed decodes cannot be replaced by direct decodes of different count numbers in the byte counter. The byte counter does not count regularly on every 1MHz logic cycle due to the operation of the resynchronising ciruit, and a 'stop' function at a certain time does not affect the progress of previously-received bytes through the delay stages.

A further decode from the byte counter indicates when address data is present, and this is used to enable the addressing circuit for the internal page request RAM. Other signals are supplied to the HOK logic, during the magazine and row address times, and to the row address and sequence number latches.

5.10. Row Addressing

Although column addressing for incoming data is always sequential, rows are directly addressable in any order. Every data line contains a row number, which determines where the data is stored in memory. If the data line is a certain type of ghost row, a further sequence number has to be taken into account when allocating addresses for storage.

The row address (and sequence number if appropriate) of an incoming data line is available as Hamming corrected data at the output of the multiplexer and is stored by pulses from the byte counter into the row address (and sequence number) latches. This information passes through the row address generator to the memory interface, normal rows being unmodified. The mapping used by the row address generator for ghost rows is described in 5.15 below.

5.11. RAM And Comparators

Four page requests at a time are possible in EURO CCT, and the numbers required are stored in RAM on the chip. Data for page requests is received through the IIC bus into register R3, and is loaded into the appropriate RAM section via the RAM data write logic.

Each of the four RAM sections has associated with it a comparator circuit. This compares the page request data coming from the RAM with the Hamming corrected data of the currently received page. If the data line is valid for the page being requested, the comparator output line will be set to a 1. Of course, it is possible for more than one comparator output line to be set simultaneously, as some incoming data may apply to a number of page requests. If the hold function has been activated, either by resetting the bit in RAM or being in the process of writing page request data, then the appropriate comparator output line is held low.

5.12. Priority Logic

The priority logic generates the chapter address for writing data to memory. For the two least significant bits (A10 and A11) the circuit basically performs a 4-line to 2-line encoding function, operating on the comparator output lines. If more than one comparator output is active, however, the priority logic applies the lowest valid address. In this way RAM and comparator 0 has priority over RAM and comparator 1, etc.

For the most significant address line (A12) the value of the 'bank select' bit (register R2 bit D6) is used in normal mode. When ghost row mode is selected, page headers and normal rows set A12 to 0, and ghost rows set it to 1. For example, if a page is selected in acquisition circuit number 1, the display data will be found in chapter 1 and any associated ghost rows in chapter 5. The signals controlling this part of the priority logic are not shown in fig. 31.

Another function of the priority logic is to ensure that the time display (last 8 characters on a page header) is always directed to the current display chapter as defined in register R4. This fact should be remembered when reading page data from memory via the IIC bus. If a memory is not the display chapter, the last 8 characters on the page header will not be written. These locations will contain spaces, or the time at which the memory ceased to be the display chapter if applicable.

A special case is also made for rolling page headers, which are directed to the display chapter by the priority logic when the page in the display chapter is being looked for. This operation is given a lower priority than writing valid page headers to other chapters, however. If pages have been requested in other chapters the corresponding headers will not roll in the display chapter, as they are required elsewhere. Only headers which are not valid for other chapters will be seen to roll. In the extreme case, where all pages are requested in other chapters (as a result of 'don't care' digit settings) rolling headers will not be obtained at all. The header will, however, turn green on a page request, and the correct page will still be received.

5.13. Page Clear Control

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The page clear control operates to erase the memory to 'space' codes for any of the four acquisition circuits. This function operates only in field flyback mode, and is disabled in full channel mode (register R1 bit D3 set to 1).

Two situations can cause page clearing in the acquisition section. The first reception of a page after a request clears the old page before writing the new page; also the broadcasters can set the C4 (erase) control bit in the page header at any time.

The clear control circuit contains the PBLF (page being looked for) flip-flops, and in combination with the comparator output lines can determine when a page has been received for the first time. Also the C4 control bit state is available to the clear control circuit (not shown in fig. 31). There are four flip-flops inside the circuit, reset every field, which store whether a clear function should take place for each of the acquisition circuits. These control the line going to the write control circuits, being enabled at the appropriate times in the field period.

When clearing, spaces are written to columns 0-39 on rows 1 to 23, and also to the corresponding ghost row chapter rows 0 to 21 when in ghost row mode. Thus if four page headers are received for the four requested pages in one field flyback period, all 8 chapters of memory may require to be cleared before the next field flyback period. This is achieved using write cycles outside the DEW (data entry window) period; the field timing being divided into 8 sections, one for possible clearing of each memory chapter.

Column addresses for page clearing are generated simply by feeding a line timing decode into the normal column counter outside the DEW period. Row addresses are specially generated by the row counter for page clearing, which supplies its output to the memory interface outside the DEW period via the multiplexer. A decode from this counter also passes to the write control circuit, to indicate when a row can be cleared.

5.14. Write Control

The write control circuit is responsible for indicating to the memory interface when a memory write cycle should be carried out. When one or more of the comparator outputs are activated, normal write cycles are enabled by the delayed decode from the byte counter to store the received data.

If clearing is required, the output from the clear control circuit together with an enable from the row counter for page clearing activate the write enable signal to the memory interface. At the same time, the clear control circuit forces the data to become a 'space' code 00100000.

The write control circuit also arranges for the time and rolling headers to be written regardless of the state of the comparator outputs. Another function is to store the magazine and channel related ghost rows, as discussed below in section 5.15. These functions are carried out with the help of the 'magazine of display chapter' circuit as explained in 5.6. above.

When the acquisition $\overline{\text{on}}$/off mode bit (register R1 bit D5) is set to 1, the write control circuit is disabled. Also all CPHR (correct page header received) flip-flops in the comparator circuits are reset. This stops erroneous pages being received when the acquisition is turned on again, in the event that a page was being received when acquisition was turned off.

5.15. Ghost Rows

Normally, EURO CCT stores 'level 1' data only (page headers and normal rows), using 1k8 of memory per page. If bit D4 in register R1 is set to 1, however, EURO CCT is capable of receiving ghost rows as well. Each page occupies 2k8 of memory in ghost row mode.

The ghost rows give optional features, and provide information for higher levels of display. Note that although EURO CCT can receive ghost rows and store them in memory for processing by the control microcomputer, this does not imply that all the ghost row facilities can be implemented. For example, a 'level 3' decoder providing parallel attributes and DRCS (dynamically redefinable character sets) will require a more sophisticated display. However, EURO CCT and suitable ghost row processing software can give the capability of multiple languages on the same page, provided the characters required are within EURO CCT's set of 128 (see section 4).

The functions of the ghost rows received by EURO CCT have been defined in a CCIR specification (reference 1). They are summarised below, together with the extent to which the functions can be implemented.

Ghost rows 24 and 25 have the same format as normal rows, containing 40 characters. In combination with rows 1 to 23 and the central 24 characters on the page header they form a page of 1024 bytes, suitable for telesoftware. They can also be used for additional page related display data, to give user control information for more sophisticated decoders. EURO CCT can deal with these applications, as the data can be read by the control microcomputer and processed or written to the display memory as appropriate.

Ghost rows 26 are used for enhanced display facilities at 'level 2' and higher levels. Using a sequence number after the row address, up to 15 different versions of ghost row 26 can be received by EURO CCT. Data is transmitted in 13 groups of 3 bytes, the first two containing special Hamming protection for address and mode description and the third comprising parity checked data. The parity checking function of EURO CCT is activated only for the parity protected bytes; a parity error here stops the byte being written to memory. Data is always written to the other bytes. In this way the normal integration of parity errors is preserved, an important feature of the 'fixed format' teletext system, while allowing Hamming protection of the addressing.

The data in row 26 is used to overwrite the 'level 1' display at any address location to enhance the display for higher level decoders. Facilities are included to define full screen and row-colours, pastel colours, accented and special characters, double height and width, underlined characters and reduced intensity. These features can be obtained as parallel attributes, without spaces between changes of function. Although EURO CCT can receive all this data, its character generator is not sophisticated enough to implement all these features. Only the multiple language data can be dealt with, within the range of the 128 character set, using the control microcomputer to read the ghost row data and write to the display memory with bit 8 set to 1. If desired, the control microcomputer can allocate the nearest available approximation to a transmitted code where the correct symbol is not available (e.g. Danish Æ replaced with Ä). EURO CCT may, however, be used as an acquisition device for a higher level teletext decoder, with processed ghost row 26 data being sent to a suitable display circuit.

Ghost rows 27 define linked page addresses. Each ghost row 27 contains 6 groups of 6 bytes, each of which specifies a page number and sub-code. A sequence number allows for four versions of row 27, so up to 24 page numbers can be linked to any given received page. The control microcomputer reads this data, and uses it in combination with user commands to determine which pages are to be searched for and displayed. Also a CRC (cyclic redundancy check) for data in the basic 'level 1' page is incorporated, allowing the control microcomputer to verify that the page is correct. This may be useful for e.g. pages with financial data. EURO CCT and suitable software in the control microcomputer can deal with all these facilities.

Ghost rows 28 are used to redefine the character set. Two types are available, distinguished by a sequence number; page related and magazine related. The page related ghost row 28 is acquired for a particular page, just like the previous ghost rows. When a magazine related ghost row 28 is received for the magazine of the display chapter, it is automatically stored regardless of the state of page requests. The magazine related ghost row 28 is always stored in memory chapter 4, whereas the page related version goes in the chapter related to the received page.

The data in ghost row 28 consists of 13 groups of 3 bytes, each group defining a character in the national option code table. As this data is Hamming protected, EURO CCT's parity checking mechanism is switched off and the data is always written. In common with other Hamming encoded data in ghost rows, the control software must provide suitable decoding. EURO CCT is capable of handling ghost rows 28 with suitable control software up to the limits of the character set, although symbol approximations can be implemented as with ghost rows 26.

Another version of ghost row 28 has been allocated in reference 1 to redefine pastel colours on a page basis, but this is not received by EURO CCT.

Ghost row 30 gives general information on the transmission, and is called the 'broadcasting service data packet'. It is transmitted about once a second on magazine 8 only, and applies to the whole transmission. EURO CCT arranges for it to be acquired always in ghost row mode regardless of page requests, and it is stored in memory chapter 4. As the data format is variable, parity checking is switched off for this ghost row.

Ghost row 30 contains information about the initial page to be acquired by the decoder without any action by the user, programme & channel labels, time in a standard format, control information and data for display. The sequence number is ignored by EURO CCT, as this is used to distinguish between multiplexed and non-multiplexed functions (field flyback and full channel data). Either will be stored, and the sequence number can be read by the control microcomputer to alter the mode in EURO CCT as appropriate. All the other features of ghost row 30 can also be dealt with by EURO CCT using appropriate control software.

All ghost rows are stored in particular locations in memory, depending on the row number and sometimes also the sequence number. Details of the address mapping are shown in fig. 32.

5.16. Full Channel Operation

In normal field flyback operation EURO CCT accepts data only during lines 6 to 22 of each field. If register R1 bit D3 is set to 1, however, data will be accepted on all t.v. lines, known as full channel operation. A data throughput rate of over 600 pages per second is possible in this mode, a very powerful technique for data distribution systems and cable t.v. networks. In full channel mode it does not matter whether the field sync sequence is retained or all lines are used for data. In the latter case the acquisition field timing will free-run, of course.

It is possible to capture normal field flyback data (multiplexed with a t.v. signal) in full channel mode but this is not recommended, as some parts of the t.v. picture are likely to be interpreted as teletext, thus corrupting the other data. If field flyback data is added to a blank t.v. channel it is safe to operate in full channel mode if required.

Note that if automatic switching between field flyback and full channel modes is required, this can be achieved using the designation code in the broadcasting service data packet (ghost row 30). In this case it is necessary to retain the field sync sequence in full channel mode, and ensure that ghost row 30 is always transmitted within the field flyback range of lines 6 to 22. This allows a decoder in field flyback mode to pick up the data, switching it to full channel operation by means of suitable control software.

General operation of EURO CCT in full channel mode is very similar to field flyback, except that automatic page clearing is no longer provided. In field flyback mode, the specification always requires one field advance warning after a page header before normal rows are transmitted for that page. Clearly this restriction is unacceptable in full channel mode as most of the transmission capacity would be wasted, so it is permissible (and usual) for normal rows to be transmitted immediately after the associated page header. In this situation there is no time to clear the memory of old data, either on first reception of a page or use of the C4 bit. Page clearing is thus deliberately inhibited when EURO CCT is switched into full channel mode.

There are two main techniques which can be used to get round this difficulty, depending on the situation. If the data is being broadcast on a reasonably secure data channel with low error rates, then the simplest solution is to transmit non-row-adaptively. In other words, all rows are sent even if they just contain spaces. Then there is no need to clear the page explicitly, as the new data can be relied upon to overwrite the old. This deals with the first reception of a new page, and the transmitter can emulate the effect of a C4 (erase) bit setting by sending a completely blank page. A minor snag with this method is that a parity error in a received character will not be displayed as a space, but the old character from the previous page will be retained. Also, due to the non-row-adaptive transmission the data is not formatted at the generator in exactly the same way as it would be for normal row-adaptive transmission.

If these restrictions are not acceptable for a particular situation an alternative solution exists. An additional page of memory is used, and on requesting a page this memory is cleared ready to receive the new data. Any parity errors will not write to the memory and will show as spaces, together with any non-transmitted rows. The other memory contains the old data, and remains displayed by the control software until the new page arrives. When this happens the control software senses the $\overline{\text{FOUND}}$ bit and then displays the new page. The memory containing the old page is now free to be cleared and used as an acquisition memory for the next page.

Note that although automatic page clearing (on first reception and with C4) is inhibited in full channel mode, the software clear page command (register R8 bit D3) still operates. It may take up to 22ms after the command before the page is cleared, the actual clearing time (after the delay) being 26 line periods (1.6ms). During the clearing time any incoming teletext data will not be written to memory, as the same memory cycles are being used to write spaces. This effect is of little consequence in this situation, as by definition the page is only cleared on a new page request when updating of the displayed page is no longer necessary.

In some full channel applications the access time may be so short that it is perfectly acceptable to clear the display memory on page request. If this is the case, the second memory and control software used to display the old page until the arrival of the new page may be dispensed with.

6. Memory Interface Function

This section describes the operation of the memory interface and suitable memory configurations for different applications.

6.1. Interface Pins

The memory interface function occupies over half of the pins of EURO CCT. This has been done for simplicity of use and to reduce interfacing components to the minimum. A block diagram of the memory interface is shown in fig. 33. The memory used is byte-wide static RAM.

There are eight data pins D0 to D7. These are bidirectional, having input buffers and three-state output buffers. They present eight bit wide parallel data to the memory for write cycles, and receive data from the memory for read cycles.

Addressing the memory is achieved through thirteen address pins A0 to A12. These are outputs only, with closed drain (push-pull) drive. Ten of these (A0 to A9) are used to access the 1024 locations within one page of memory, known as a 'chapter'. The remaining three pins (A10 to A12) address up to eight memory chapters. Address A12 is used to distinguish between normal and ghost row data in ghost row mode, and in normal mode is the pin activated by the 'bank select' bit in the acquisition circuit.

The control pin $\overline{OE}$ (output enable) is activated (low) whenever data is to be read from the memory. It should be connected to the corresponding pin of the memory devices to enable their three-state buffers. As EURO CCT's three-state buffers are not enabled when $\overline{OE}$ is low, the direction of data flow can be reversed without bus conflicts.

Finally a write enable pin ($\overline{WE}$) is active low when data has to be written into memory.

6.2. Memory Cycles

Various functions need to be performed by the memory interface. Received teletext data must be written to memory, and read from memory to drive the display. Data travelling down the IIC bus may be written to or read from the memory. Also other special write and read functions are necessary to operate the circuitry in EURO CCT.

Referring to fig. 33, the memory timing generator allocates times for performing all the various functions. It controls various multiplexers which ensure that the correct addresses (and data also for a write cycle) are output for each function. Column and row addresses are passed through an address mapping circuit, equivalent to the adder device in the first generation LSI decoder.

Also included in the memory interface is a cursor enable circuit, see 6.6.

The fundamental principle governing the design of the memory interface is the requirement to write and read teletext data simultaneously during the same t.v. line period. This is necessary for non-interlaced display and full channel operation. The line period of 64us is divided into 128 periods of 500ns, each being used for one memory cycle. Alternate memory cycles are write and read, so that write cycles always start an integral number of microseconds after line sync. Read cycles always start on the half microsecond points. These characteristics are shown in fig. 34.

Fig. 34 also shows the sequence of events within the individual write and read cycles. For details of the timings see the EURO CCT system specification.

6.3. Read Cycles

****

The cycles used for the read function are shown in fig. 35. Forty cycles every line are used to read display data; this includes the page attributes mentioned in section 4.3.

A further two cycles are allocated for reading IIC bus data. Although the maximum data rate on the IIC bus of 100kHz corresponds to less than one byte read per line period, two reads are necessary to ensure that data from the memory is loaded into the IIC interface in sufficient time.

The remaining 22 read cycles in the line are unused.

6.4. Write Cycles

****

The cycles used for the write function are shown in fig. 36. Sixty of the cycles per line are write cycles for teletext acquisition.

Although only forty bytes need to be written for each data line, they occupy 46us at the standard 6.9375Mb/s data rate. A further 1.4us tolerance in the data position and delays in the VIP2, line locking and resynchronising in EURO CCT increase the uncertainty of the output data position in the line. In addition when a page header arrives a further two write cycles are necessary for magazine number and PBLF resetting. Allowing for 60 possible write cycles permits all these tolerances to be accommodated, although for any given line only 40 (or 42) will be used.

One write cycle is sufficient to service the IIC bus at its maximum speed of 100kHz.

A write cycle is allocated for setting the PBLF (page being looked for) function, see 5.5. This is only used for setting the function on a page request; resetting the function is performed by another cycle in the acquisition group on reception of a page header as mentioned above.

Finally, a write cycle is allocated for inserting the colour control character (alphanumerics white or green) in row 0 column 7 of the display chapter. This gives the green rolling header function as described in section 5.

One remaining write cycle on the line is unused.

For page clearing, 40 consecutive write cycles in the acquisition group are used to write spaces in a row. The lines used for clearing (synchronised to the acquisition timing chain) are shown in fig. 37. Only the software clear function is enabled in full channel mode. Line numbers shown in fig. 37 refer to the first part of the function: in fact the clear write cycles start at 45us through the line indicated and continue until 20.5us into the following line.

6.5. Address Mapping

Although any location in a memory chapter is addressed by column (0 to 39) and row (0 to 25), EURO CCT includes an addressing circuit to map these into one of 1024 locations via address lines A0 to A9. The algorithm used is not the same as the (column + 40 * row) method of the adder in the first-generation LSI decoder. Instead a multiplexing arrangement gives addresses following the row number if the column number is less than 32. When the column is 32 or greater, the address lines inverted are shifted to different outputs in such a way that the address counts down from the maximum of 1023 in groups of 8. The arrangement and address map are shown in fig. 38.

All 1024 addresses (0 to 1023) can be addressed by this arrangement. The highest valid input address is row 25 column 23. It is possible, however, to set higher addresses into the IIC registers, e.g. by software error. If the address applied is invalid an out of range signal is obtained, which inhibits the write control circuit. This prevents erroneous data being written to the memory.

6.6. Cursor Enable Circuit

Although it is not directly involved in addressing the memory, the cursor enable circuit is included in the memory interface function because of the proximity of the necessary signals. The object of the cursor enable circuit is to determine when the cursor address (as determined by the active row and column addresses in registers R9 and R10) is coincident with the location being scanned by the character generator.

As can be seen from fig. 33, the row and column addresses are compared in two comparators. If both comparisons are valid, a delayed cursor enable signal is passed to the character generator. This allows the background and foreground colours to be reversed if the cursor function is switched on. The delay unit compensates for the time taken to address the memory, read the data and access the character generator ROM.

Note that only row and column addresses are compared; no account is taken of the chapter address. It is therefore possible to see the cursor display on the screen even if active data through the IIC bus is being written to or read from another memory. The control software must define the required function and switch off the cursor if this mode of operation is not required.

6.7. Memory Configurations

Interfacing the memory for most applications is straightforward. Standard 'byte-wide' static RAM is used, and up to 8k8 may be connected directly in 1k8 steps. If one memory device is sufficient for the requirement (either 1k8, 2k8, 4k8 or 8k8 sizes) no interfacing components are necessary, as shown in fig. 39.

When more than one memory device is used a selector circuit may be necessary to convert the chapter address lines (A10 to A12) to chip select signals. Such an arrangement is shown in fig. 40 where four 2k8 memory devices are used in an 8 page decoder.

Where smaller amounts of memory are being used, some or all of the chapter address lines A10 to A12 may be left unconnected. Note that A12 is the selector between normal and ghost row data, as explained in section 5. With 2k8 of memory, A12 would be connected to the A10 pin of the RAM device if a single page ghost row decoder were required. However, A10 would be used instead for a two page decoder without ghost rows.

It would be possible to connect more than 8k8 of RAM to the memory interface, using e.g. microprocessor port pins as additional inputs to the memory selector circuit. However, it would only be possible to select one bank of 8k8 memory at a time both for acquisition and display purposes, as the microprocessor would be unable to switch at the correct time or quickly enough to separate these functions. Also the maximum loading on the EURO CCT pins should not be exceeded. However, with suitable buffering the technique might suit applications where a larger number of pages are needed in reserve without having to be updated.

As mentioned in section 2, another possible configuration might include a parallel bus interface to e.g. a home computer for telesoftware. The basic question to be decided here is whether the interface needs to operate at the same time as data is actually being received or not. If not, three state buffer devices between the EURO CCT address and data pins and the memory circuit may be all that is necessary. The buffers could be controlled by a port pin on a microcoputer, the software arranging for the memory to be disconnected from EURO CCT when e.g. a page of telesoftware has been received and is ready for transfer.

If "simultaneous" operation of the bus interface and data reception is essential, a more complex interfacing circuit must be designed which can allocate memory cycles for transfer so that they do not conflict with the active EURO CCT memory cycles described in this section. In considering such a circuit, it should be carefully studied whether the performance it will provide is worth the complexity. Factors to be borne in mind are the limited number of spare memory cycles, and reduction in speed of a microcomputer interface due to setting up and incrementing addresses, etc. It may well be found that an adequate performance can be achieved by simply reading data through the IIC bus. This eliminates RAM interfacing hardware, and also may simplify transfer due to the automatic address generation and incrementing.

7. IIC Interface And Control Functions

This section describes the IIC interface and how it can be used to control the operation of EURO CCT.

7.1. Interface Pins

Two pins are used to interface EURO CCT to its controlling microcomputer. The IIC bus is a serial communication system, and requires serial data SDA and associated data clock SCL. As EURO CCT is a slave transceiver, the data clock is always generated by the microcomputer and the SCL pin is an input only. The SDA pin, however, is an input and open drain output as data can flow down the IIC bus in either direction.

The IIC signals are intended to be driven from open drain or open collector sources with suitable pull-up resistors to the +5V supply line.

7.2. Control Functions

As indicated in sections 1 and 2, one of the major design considerations for EURO CCT is to obtain the maximum flexibility in use. This is achieved through software variations in the control microcomputer, communicated to EURO CCT via the IIC bus.

The following general categories of control function are available in EURO CCT. Depending on the application, some or all of these functions need to be performed by the control microcomputer.

(a) Writing to EURO CCT:-

1. Selection of function (acquisition on/off, full channel etc).
2. Display control (text on/off, interlace, double height etc).
3. Display chapter selection.
4. Requesting a page.
5. Writing data to memory for display.

(b) Reading from EURO CCT:-

1. Reading memory for status of system (found, etc).
2. Reading memory for page related data (page no., control bits, etc).
3. Reading memory for display data (e.g. for recording).
4. Reading memory for ghost row data (for processing).

Write commands to EURO CCT load data as required into the control registers R1 to R10, or write data to memory via R11. When reading from EURO CCT, only the memory can be read, not the state of the control registers. If it is necessary to remember the state of a bit in a register for software control purposes, a record must be kept in a register in the microcomputer.

7.3. IIC Command Structure

The operation of the IIC bus is described fully in reference 3. Operating speeds from 0 to 100k bits/second are allowed, and the system allows multi-master operation with arbitration in case of simultaneous access to the bus. Also the transmission rate is automatically controlled to suit the slowest device in a configuration.

The IIC interface in EURO CCT is a slave transceiver capable of going at the maximum speed, so the rate of data transfer is dependent on the control microcomputer. The clock SCL is always provided by the microcomputer whether it is writing to, or reading from, EURO CCT. Only the microcomputer can initiate data transfer down the IIC bus, not EURO CCT.

It is possible to generate the IIC protocol on two port pins of almost any standard microcomputer. However, this may take more software (ROM space) than is convenient and speed is likely to be greatly restricted. The use of the MAB8400 series of microcomputers is recommended, as the hardware interface they incorporate greatly simplifies generation of IIC commands.

Three basic types of command are allowed, as shown in fig. 41. In all of these the transmission commences with a start condition STA, followed by an optional start byte. The latter is for use in low speed mode, to allow a slow receiving processor time to take action. EURO CCT will operate whether the start byte is present or not at any speed.

Following the start condition is the slave address, which is used by the control microcomputer to indicate that the command is for EURO CCT and not another device connected to the same bus. The EURO CCT slave address is fixed at 0010001 (mask programmable). EURO CCT does not respond to the 'general call' address (see ref. 3).

Immediately following the 7 bit slave address is a single bit, write or read, which indicates the direction of data flow. If it is set to read, the data output buffer on EURO CCT will be turned on for the next and subsequent bytes until the processor ends the sequence by not acknowledging the last data byte. This is to avoid conflicts in the generation of the stop condition. If the read/write bit is set to write, the EURO CCT data output buffer remains off except to acknowledge each data byte received from the control microcomputer.

Every transmision writing to EURO CCT contains a single byte sub-address following the slave address. This sub-address selects the register required (R1 to R11), and sets up the address pointer. The address pointer may, however, increment later on subsequent byte transmissions, see 7.4. below.

When reading data from EURO CCT, external memory will always be read. If the address pointer is set to R11, the memory address will increment. No incrementing takes place if the address pointer is set to any other register value. Note, however, that if R8, R9 or R10 are selected the address pointer will auto-increment to R11 later as described in 7.4 below. The IIC command may just read EURO CCT, with the address pointer remaining at the location set up by a previous transmission as shown in fig. 41(b). Alternatively, the address pointer may be set up and data read in one IIC command as shown in fig. 41(c).

The number of data bytes in a transmission is, in general, unlimited. However, if slow speed mode is chosen, the number of bytes should be limited to six to conform to the IIC bus specification.

7.4. Auto Increment

All registers in EURO CCT can be directly addressed by the sub-address. However, to transmit a new sub-address the IIC command must stop and start up again, as the sub-address is defined to be the second byte after the start condition. Some combinations of mode registers are often set up together, so EURO CCT incorporates an auto increment facility. After data has been loaded into certain registers, the address pointer is incremented to address the next register. If a further data byte is transmitted it will be loaded into the new register. This allows several registers to be simply loaded in one IIC bus transmission with minimum overheads.

When register R11 is written, the memory address increments after writing data. Since the active chapter, row and column registers R8, R9 and R10 auto increment also, it is possible to write a string of characters to memory in one IIC transmission. Example transmission sequences are shown in fig. 42.

Note that the address pointer auto increments for read as well as write bytes. This is only of relevance when considering special sequences for reading data from RAM, as normally R11 will be selected which does not auto increment.

7.5. R1 Mode Register

This has sub-address 00000001.

	$\overline{7+P}$/	ACQ.	GHOST	$\overline{DEW}$/	TCS			
TA	8 Bit	$\overline{ON}$/OFF	ROW	FULL	ON	T1	T0	R1
			ENABLE	FIELD				

All bits in this register are set to 0 on power-up.

This register contains mode controls for various functions, and should be set up by the control microcomputer as required. Some functions may change from time to time in the same system.

T1,T0
***** These bits determine the display timing as follows:

00	interlaced 312/313 lines
01	non-interlaced 312/313 lines*
10	non-interlaced 312/312 lines*
11	timing slaved from another sync source

*These modes will be inhibited if a newsflash or subtitle is being displayed. See 3.4.

TCS ON
****** A 1 on this bit turns on the $\overline{TCS}$/$\overline{SCS}$ output buffer, providing TCS (text composite sync) from EURO CCT as defined by T1,T0 above. When used in the normal way with VIP2 (SAA5230) this bit determines whether sync to TV is TCS (TCS ON = 1) or broadcast sync (TCS ON = 0). See 3.8.

$\overline{DEW}$/FULL FIELD
********** A 0 on this bit selects field flyback operation, with DEW (Data Entry Window) between lines 6-22 inclusive. A 1 on this bit selects full channel operation, with data allowed on every line. See 5.16.

GHOST ROW ENABLE
********** For normal operation this bit is a 0 and one chapter (1k8) of memory is used for each page. When the bit is set to a 1, two chapters (2k8) are allocated per page and ghost rows can be received as well as normal page data. See 5.15.

ACQ.$\overline{ON}$/OFF
********** When this bit is a 0 the acquisition circuit operates normally. If it is set to 1, the entire acquisition function is turned off, e.g. for viewdata mode or telesoftware display. The software page clear command still operates, however. See also 5.14.

$\overline{7+P}$/8 BIT
********* Normal 7 bit plus-parity reception of data is selected when this bit is 0. A 1 causes all 8 bits to be stored in the memory and the parity check is disabled. Hamming encoded data is stored in the usual way in both modes. If 8 bit mode is chosen, the data will probably have to be processed to make an intelligible display. See 5.8.

TA
** This is a mode bit for testing purposes which must be set to 0 for normal operation.

This register address increments (after one byte of data) to R2.

7.6. R2 Page Request Address Register

This has sub-address 00000010.

	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	
-								R2

All bits in this register are set to 0 on power-up.

This register contains addressing information relating to a request for a page. It will be accessed by the control microcomputer when a new page is requested.

START COLUMN SC2,SC1,SC0
These three bits are set up to indicate which column in the on-chip page request RAM should be addressed first on a subsequent write to register R3. See 5.4.

TB
This is a mode bit for testing purposes which must be set to 0 for normal operation.

ACQ.CCT A1,A0
These two bits determine which of the four acquisition circuits is being selected for a page request. They correspond to address lines A11 and A10 respectively for subsequent reception of the page. See 5.4.

BANK SELECT A2
In normal (not ghost row) mode this bit selects which bank of four memory chapters is being addressed for acquisition. It corresponds to address line A12 for subsequent reception of the page. See 5.4.

This register address increments (after one byte of data) to R3.

7.7. R3 Page Request Data Register

This has sub-address 00000011.

			PRD4	PRD3	PRD2	PRD1	PRD0	
-	-	-						R3

This register receives data for page requests. It is written by the control microcomputer when requesting a new page.

PRD4 to PRD0
********** These five bits represent the data which is stored in the on-chip page request RAM. They are written sequentially by the microcomputer, starting at the column determined by the 'start column' bits previously set up in register R2. The format of the data is shown in fig. 27. See also 5.4. and fig. 28.

This register address does not increment to another register. This is because subsequent bytes of data cause the column of the on-chip page request RAM to be incremented.

All locations in the page request RAM's are cleared to 0 on power-up. This effectively means that the acquisition circuits are on 'hold', with no pages being requested until a command is received from the microcomputer. Also, all digits are "don't care", so that subsequent normal page requests need not address the sub-code digits.

7.8. R4 Display Chapter Register

This has sub-address 00000100.

-	-	-	-	-	A2	A1	A0	R4

All bits in this register are set to 0 on power-up. This register will be written by the control microcomputer in a multipage decoder as a result of user commands.

A2,A1,A0
******** These three bits are used to select which of the eight memory chapters is to be used for display. They correspond to the logic states on the address pins A12 to A10 respectively during memory read cycles.

This register address increments (after one byte of data) to R5.

7.9. R5 Display Control Register (Normal)

This has sub-address 00000101.

BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5

On power-up, PON OUT and PON IN are set to 1. All other bits are set to 0.

The functions controlled by this register are in two groups; those applicable inside the boxing function (IN) and outside the boxing function (OUT). This register is used to control the display only when the page is not a newsflash or a subtitle, i.e. control bits C5 and C6 are both 0.

PON IN, PON OUT
********** These bits determine whether the t.v. picture is on inside and outside the boxing function respectively. This function is controlled via the BLAN pin (high to blank t.v. picture). A 1 in the register means t.v. picture on, a 0 means t.v. picture off. The background function has priority over these bits, see 4.6.

TEXT IN, TEXT OUT
********** These bits determine whether text is to be displayed inside and outside the boxing function respectively. A 1 means text on, and a 0 means text off.

COR IN, COR OUT
********** These bits determine whether the contrast of the t.v. picture is to be reduced inside and outside boxes respectively. A 1 means reduced contrast, and a 0 means normal contrast. This function is controlled via the COR pin, see 4.6.

BKGND IN, BKGND OUT
********** These bits determine whether any text displayed is both foreground and background colours, or foreground colours only, inside and outside the boxing function respectively. A 1 means both foreground and background colours, and a 0 means foreground colours only. This function has priority over the PON function, see 4.6.

Examples of the use of these controls are shown below:

(a)	| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |	gives t.v. picture only, with no text allowed.
(b)	| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |	gives text only.
(c)	| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |	gives a mixed t.v. picture and text display, with a reduced contrast picture and box control characters ignored.
(d)	| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |	gives t.v. picture, with text in reduced contrast picture boxes (improved subtitle mode).

For further information on the use of these controls see 4.6.

This register address increments (after one byte of data) to R6.

7.10. R6 Display Control Register (Newsflash/Subtitle)

This has sub-address 00000110.

BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6

On power-up PON OUT and PON IN are set to 1. All other bits are set to 0.

This register is identical in structure and function to R5, but is used whenever the page to be displayed is a newsflash or a subtitle. Either C5 or C6 in the display chapter must be a 1.

The provision of two display control registers R5 and R6 allows the control mirocomputer to set up the functions required for both types of page in advance. When the type of page changes the display will be controlled automatically and there is no need for the control microcomputer to intervene.

This register address increments (after one byte of data) to R7.

7.11. R7 Display Mode Register

This has sub-address 00000111.

STATUS ROW $\overline{\text{BTM}}$/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$/REVEAL	$\overline{\text{TOP}}$/BOTTOM	$\overline{\text{SINGLE}}$/DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7

All bits in this register are set to 0 on power-up.

This register will be written by the microcomputer as required before text is displayed. It may also be written as a result of user commands.

BOX ON 0
******** A 1 on this bit enables the boxing function on row 0. See below.

BOX ON 1-23
********** A 1 on this bit enables the boxing function on rows 1 to 23 inclusive. See below.

BOX ON 24
********* A 1 on this bit enables the boxing function on row 24.

The box function controls are intended to give flexibility for on-screen status displays. Their action depends on the presence of boxing control characters and the states of the display control registers R5 or R6 as appropriate. For example, the control software may insert boxing control characters in row 24 for status displays. For a subtitle display, the subtitle may be displayed without the status box by setting BOX ON 1-23 to 1 and BOX ON 24 to 0. Conversely, a status display for television mode could be obtained by setting BOX ON 24 to 1. Ensuring that BOX ON 1-23 was set to 0 would prevent the display of any newsflash or subtitle that happened to be stored in the page memory. See also 4.6.

$\overline{\text{SINGLE}}$/DOUBLE HEIGHT
********** A 0 in this bit selects normal (single height) characters, and a 1 selects a double height character display. The display of row 24 remains in single height characters always. See 4.5.

$\overline{\text{TOP}}$/BOTTOM
********** A 0 in this bit selects top half of page, rows 0 to 11, and a 1 selects bottom half of page, rows 12 to 23, when double height is activated. In single height the state of the bit is irrelevant.

$\overline{\text{CONCEAL}}$/REVEAL
********** A 0 on this bit allows conceal control characters to take effect, displaying areas of text as spaces. The effect of the conceal control characters is disabled when the bit is set to a 1.

CURSOR ON
********* When this bit is set to 1 the cursor is displayed at the active IIC address position, provided it is within the display address range. A 0 on this bit turns the cursor display off. A flashing cursor can be obtained by writing repetitively to this bit. See 4.4. and 6.6.

STATUS ROW $\overline{\text{BTM}}$/TOP
********** Row 24, the status row, is displayed below the main text display area when this bit is a 0. When the bit is a 1, it is displayed above the main text area (i.e. display starts with row 24, followed by row 0,1,.....23).

This register address does not increment, being at the end of the display control functions.

7.12. R8 Active Chapter Register

This has sub-address 00001000.

-	-	-	-	CLEAR MEMORY	A2	A1	A0	R8

On power-up, A0 to A2 are set to 0.

This register will be accessed by the control microcomputer when writing data to, or reading from, the page memory.

A2,A1,A0
******** These three bits select the chapter to be accessed via the IIC bus. They correspond to address pins A12, A11 and A10 respectively. This chapter address is entirely independent of the chapters chosen for display (in R4) and acquisition (in R2).

CLEAR MEMORY
************ This bit in the register is not latched, as it is a transient function. When a 1 is written to this bit, the memory chapter addressed in this register is cleared. The 'space' code 00100000 is written to all memory locations from row 0 column 0 to row 25 column 23. This function may take up to 22ms after receipt of the command. See 5.16 and 6.4.

This register address increments (after one byte of data) to R9.

7.13. R9 Active Row Register

This has sub-address 00001001.

-	-	-	R4	R3	R2	R1	R0	R9

On power-up, all bits in this register are set to 0.

This register will be accessed by the control microcomputer when writing data to, or reading from, the page memory.

R4....R0
******** These five bits contain the row address to be accessed via the IIC bus. Addresses 26 to 31 inclusive can be set into the register, but are outside the valid address range, see 6.5.

The row address will increment automatically when the active column goes from 39 to 0. Row 23 increments to row 0. Rows 24 and 25 can only be selected by direct write to this register. Rows 24 to 31 increment also to row 0 (return to valid address as soon as possible after out of range address). This register address increments (after one byte of data) to R10.

7.14. R10 Active Column Register

This has sub-address 00001010.

-	-	C5	C4	C3	C2	C1	C0	R10

On power-up, all bits in this register are set to 0.

This register will be accessed by the control microcomputer when writing data to, or reading from, the page memory.

C0....C5
******** These six bits contain the column address to be accessed via the IIC bus. Addresses 40 to 63 inclusive can be set into the register, but are outside the valid address range, see 6.5. The column address will increment automatically after each read or write to the active data register R11. Column 39 increments to column 0. Also columns 40 to 63 increment to column 0 (return to valid address as soon as possible after out of range address.)

This register address increments (after one byte of data) to R11.

7.15. R11 Active Data Register

This has sub-address 00001011.

D7	D6	D5	D4	D3	D2	D1	D0	R11

This register will be accessed by the microcomputer when writing data to, or reading from, the page memory.

D7....D0
******** These eight bits are the data stored in the memory location selected by the active chapter, row and column registers R8, R9 and R10. The bits in R11 are read/write, so the data already in the memory can be read down the IIC bus by a read command. Also new data can be written to the memory from the IIC bus by a write command.

Each write or read to this register increments the column (and sometimes row) address as noted above, allowing the transfer of strings of data bytes in one IIC bus transmission. See 7.3. and 7.4.

The data written to or read from the memory performs various functions depending on the addresses chosen. In particular it is worth remembering the page attribute data stored in row 25; see fig. 29. If the C10 control bit (inhibit display) is set to 1, the page will not be displayed whatever other control functions may be set up.

This register address does not increment of itself to another register, since successive writing of data increments the active column (and row) as explained above.

7.16. Register Map

For ease of reference, the full register map is summarised below.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
T_A	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	GHOST ROW ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T_1	T_0	R1 MODE
–	BANK SELECT A_2	ACQ. CCT A_1	ACQ. CCT A_0	T_B	START COLUMN SC_2	START COLUMN SC_1	START COLUMN SC_0	R2 PAGE REQUEST ADDRESS
–	–	–	PRD_4	PRD_3	PRD_2	PRD_1	PRD_0	R3 PAGE REQUEST DATA
–	–	–	–	–	A_2	A_1	A_0	R4 DISPLAY CHAPTER
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5 DISPLAY CONTROL (NORMAL)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6 DISPLAY CONTROL (NEWSFLASH/SUBTITLE)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7 DISPLAY MODE
–	–	–	–	CLEAR MEMORY	A_2	A_1	A_0	R8 ACTIVE CHAPTER
–	–	–	R_4	R_3	R_2	R_1	R_0	R9 ACTIVE ROW
–	–	C_5	C_4	C_3	C_2	C_1	C_0	R10 ACTIVE COLUMN
D_7 (R/W)	D_6 (R/W)	D_5 (R/W)	D_4 (R/W)	D_3 (R/W)	D_2 (R/W)	D_1 (R/W)	D_0 (R/W)	R11 ACTIVE DATA

T_A and T_B must be 0 for normal operation.
All registers are write only, except R11 (Read/Write).
All bits in registers R1 to R10 are cleared to 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to 1.

All memory is cleared to 'space' (00100000) on power-up, except row 0 column 1 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is on.
– bit does not exist.

8. References

1. " Characteristics of Teletext Systems "

   Vol. 11 Report 957, CCIR XV Plenary Session Geneva 1982.

2. " IIC Bus in Consumer Applications "

   Technical Publication M83-0196, Mullard Limited 1983.

3. " Serial Data Buses ", introduction to Mullard Technical Handbook,

   Book 4, Part 3. September 1982.

4. " User Instructions for the Serial I/O Interface of the MAB8400

   Series of Microcomputers " Philips Technical Publication 022,

   5 October 1981.

5. EURO CCT SAA5240 System Specification / data sheet.

6. VIP2 SAA5230 Specification / data sheet.

7. MAB8400 series microcomputer data sheet.

9. Index

10. List of Figures

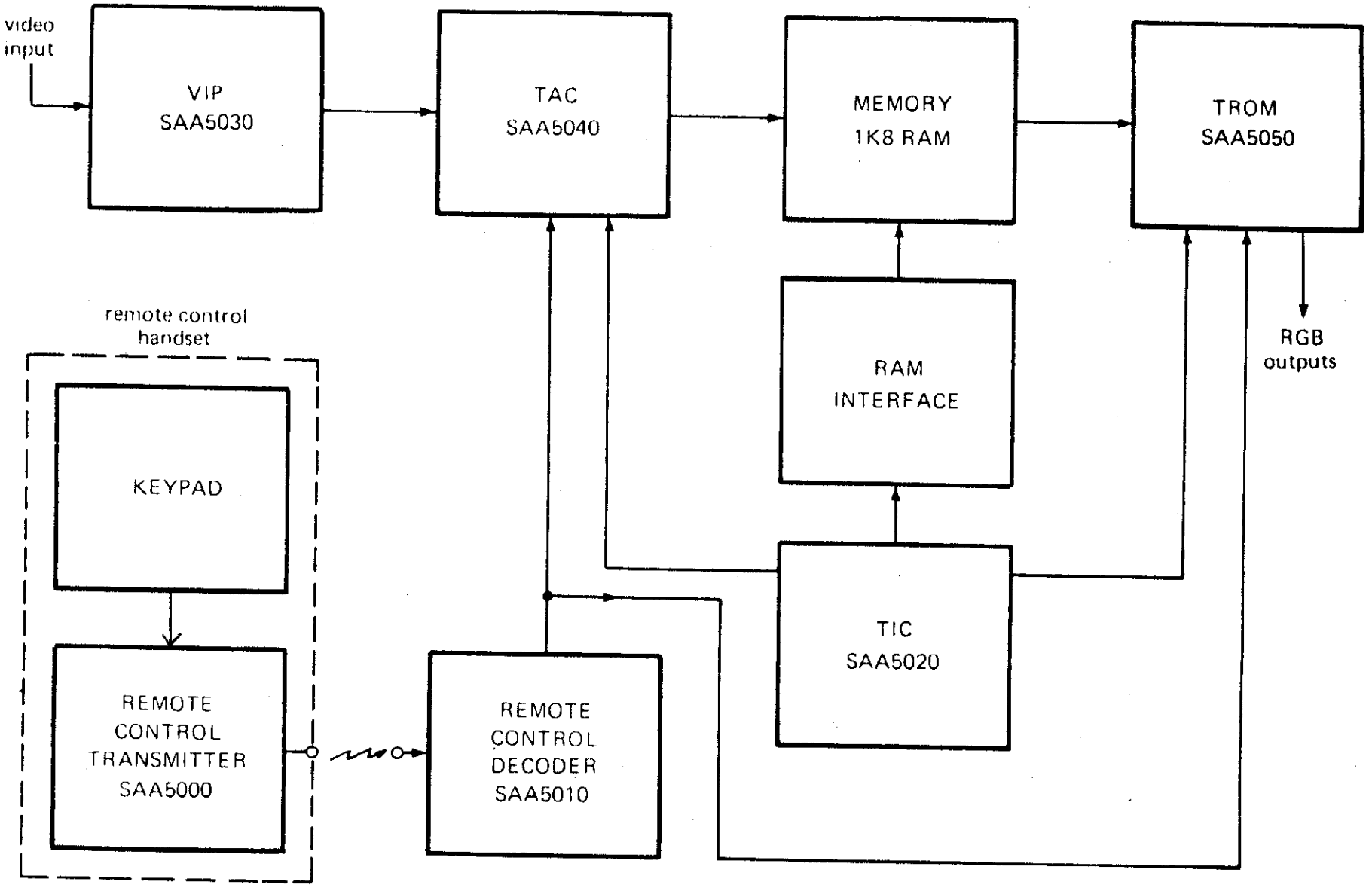


FIG. 1 THE FIRST GENERATION LSI DECODER

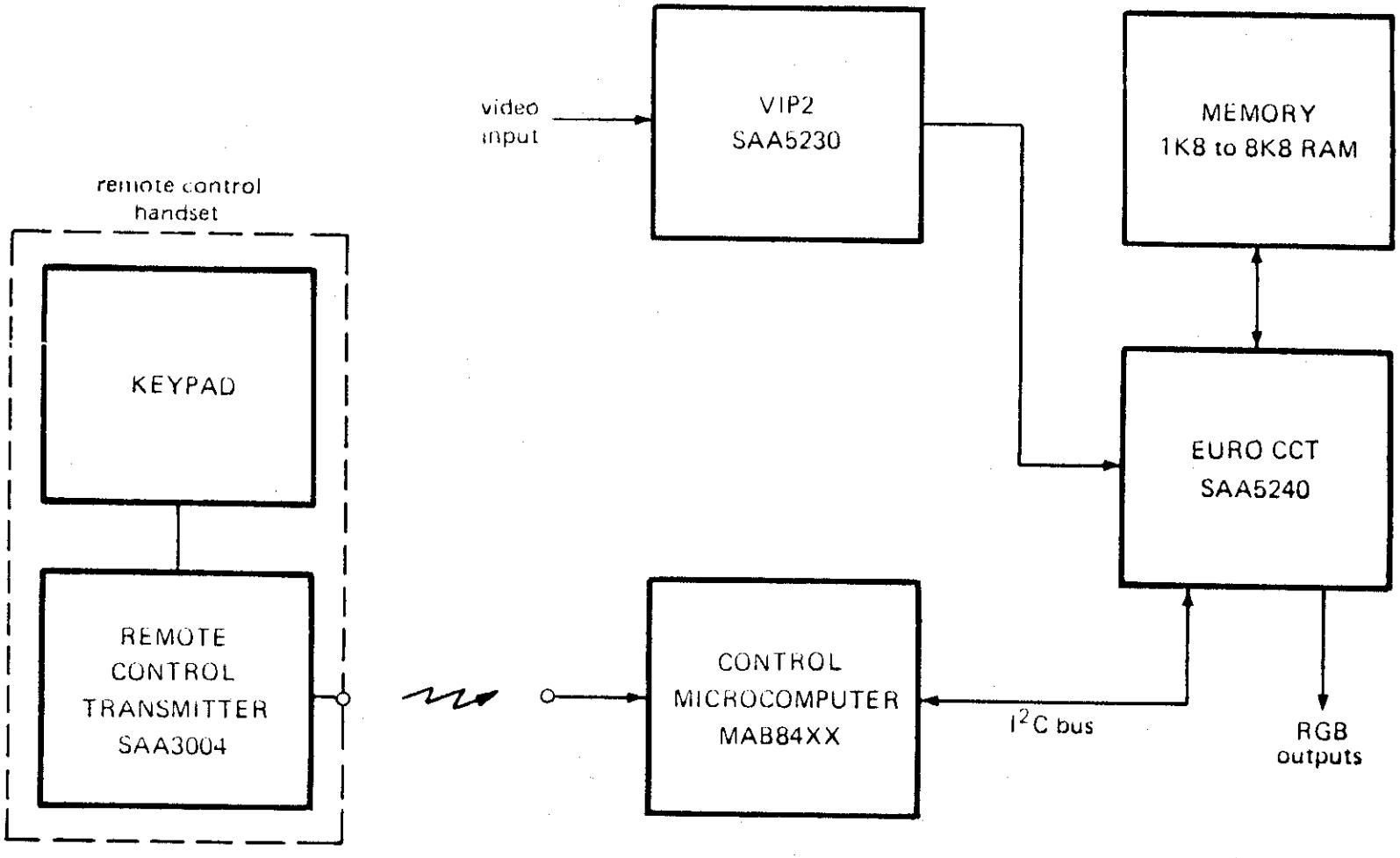


FIG. 2. THE EURO CCT-BASED DECODER

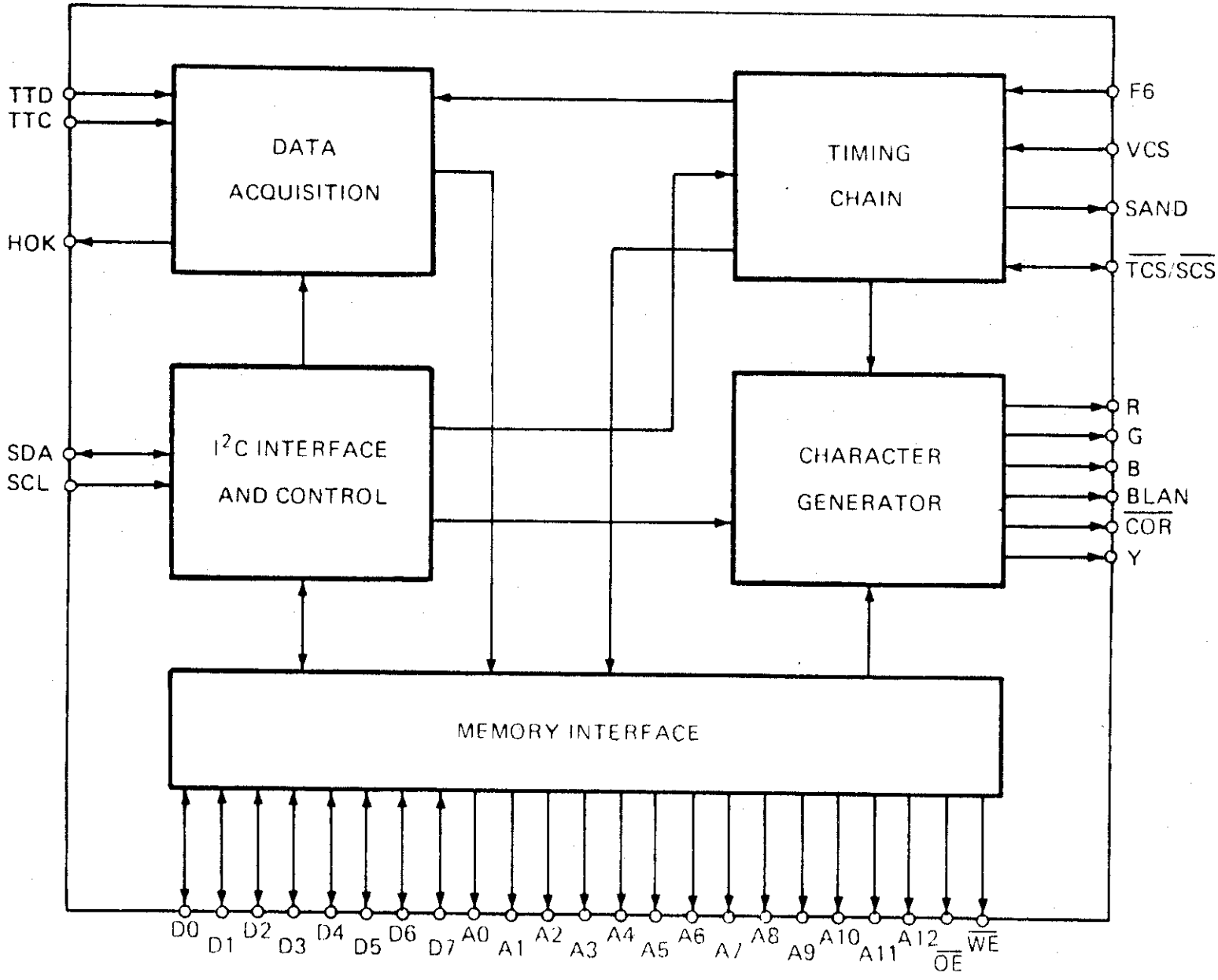
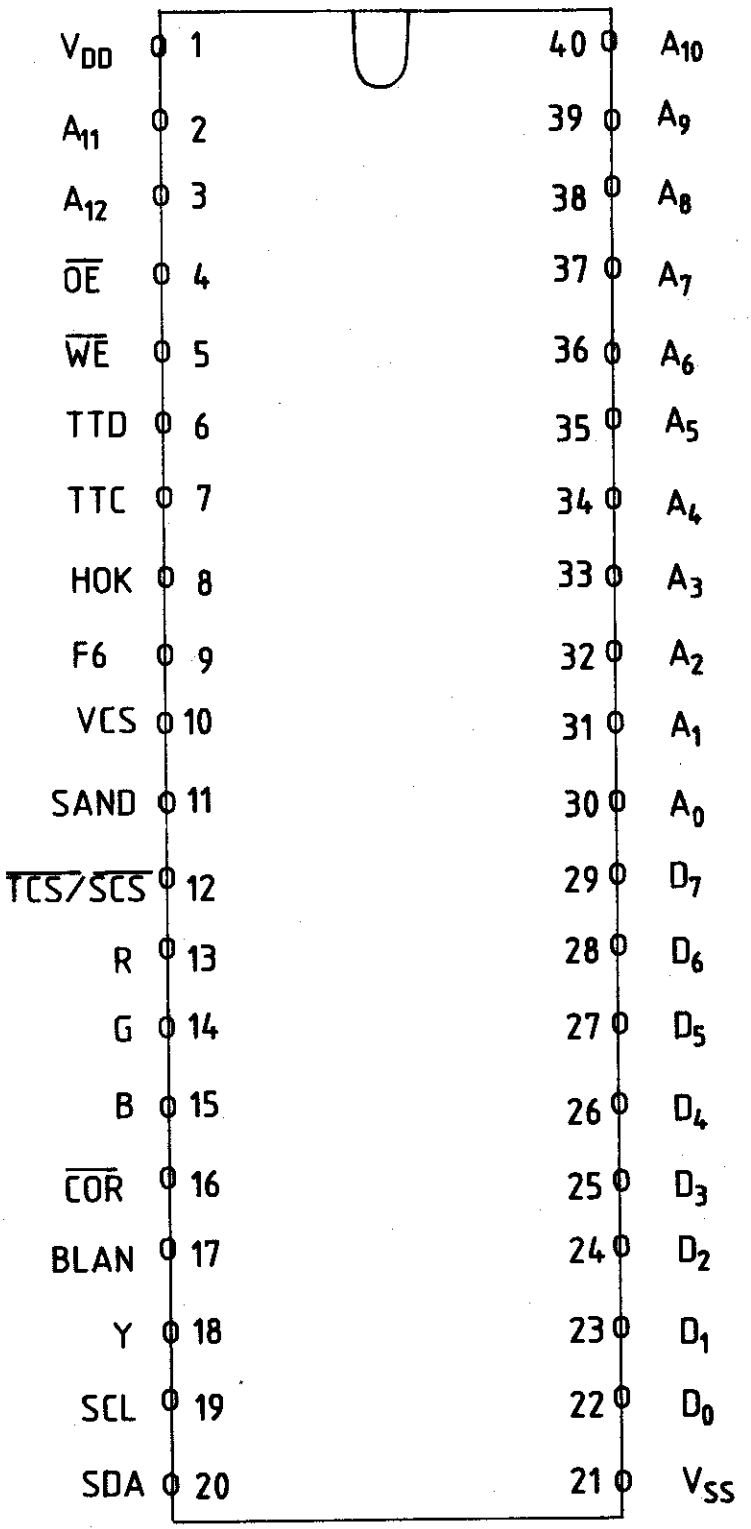


FIG. 3. EURO CCT BLOCK DIAGRAM



VIEWED FROM TOP

FIG. 4 EURO CCT PINNING

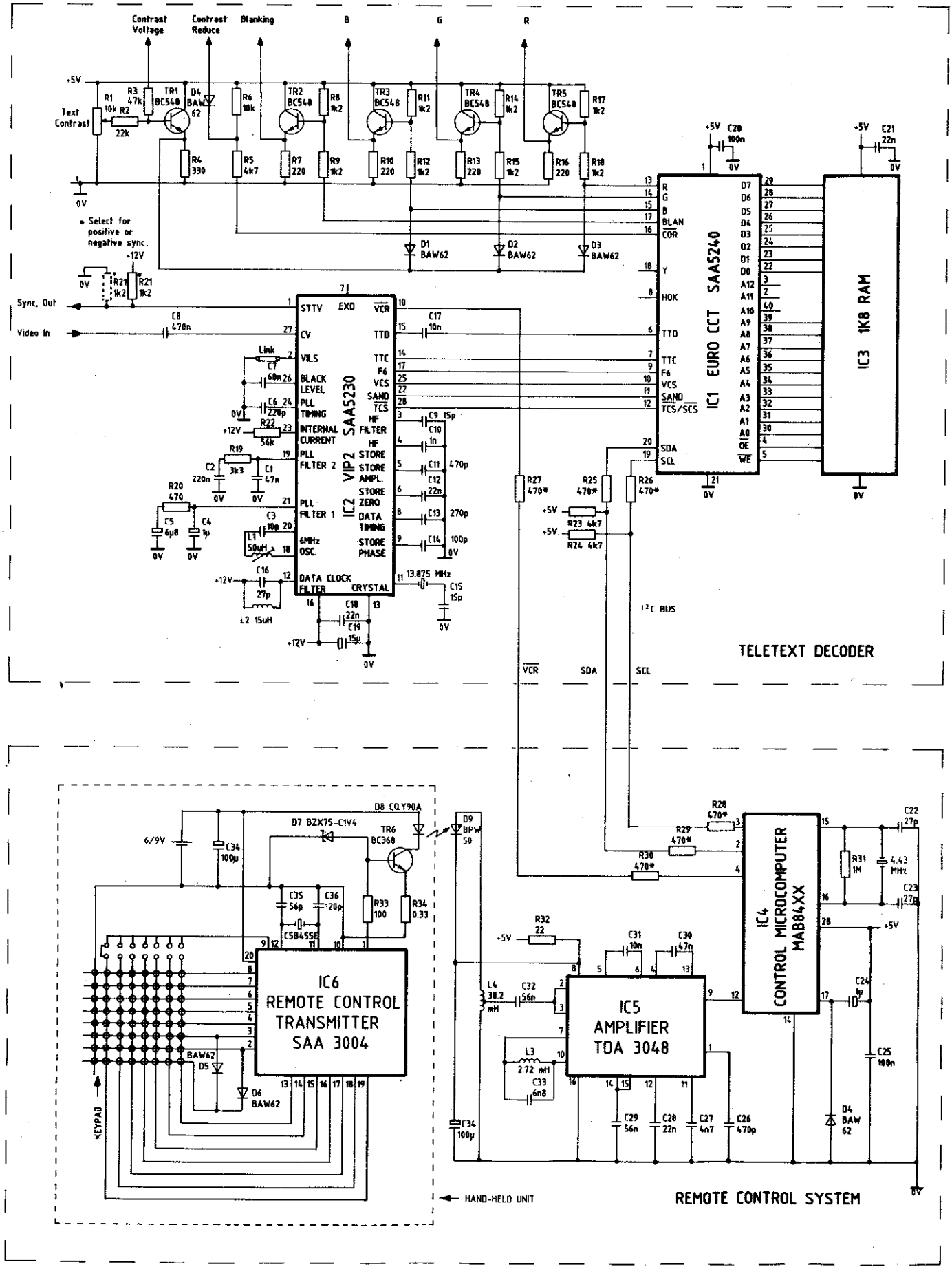


FIG. 5 SINGLE PAGE TELETEXT DECODER AND REMOTE CONTROL SYSTEM

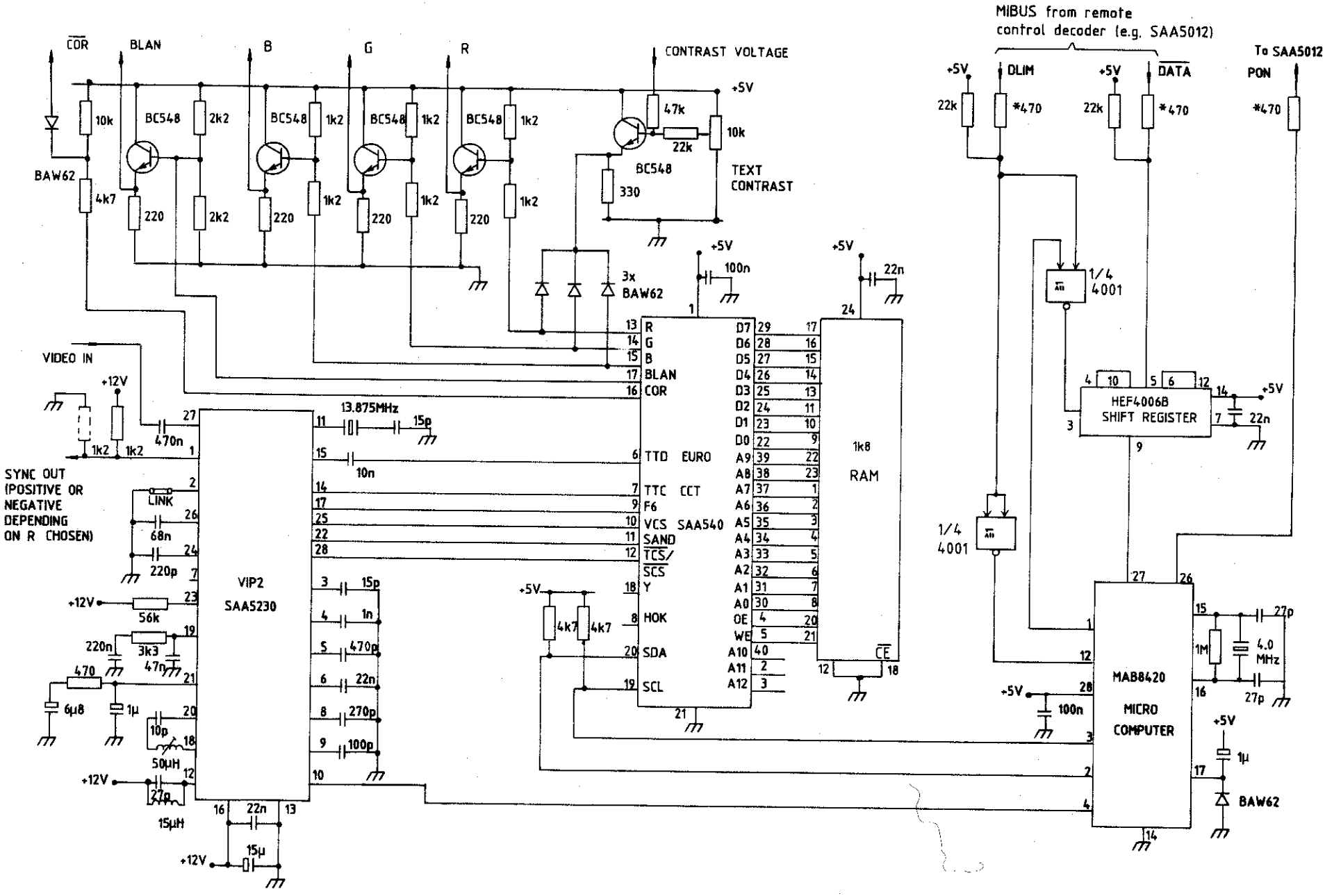


FIG. 6 FUNCTIONAL REPLACEMENT FOR LSI DECODER

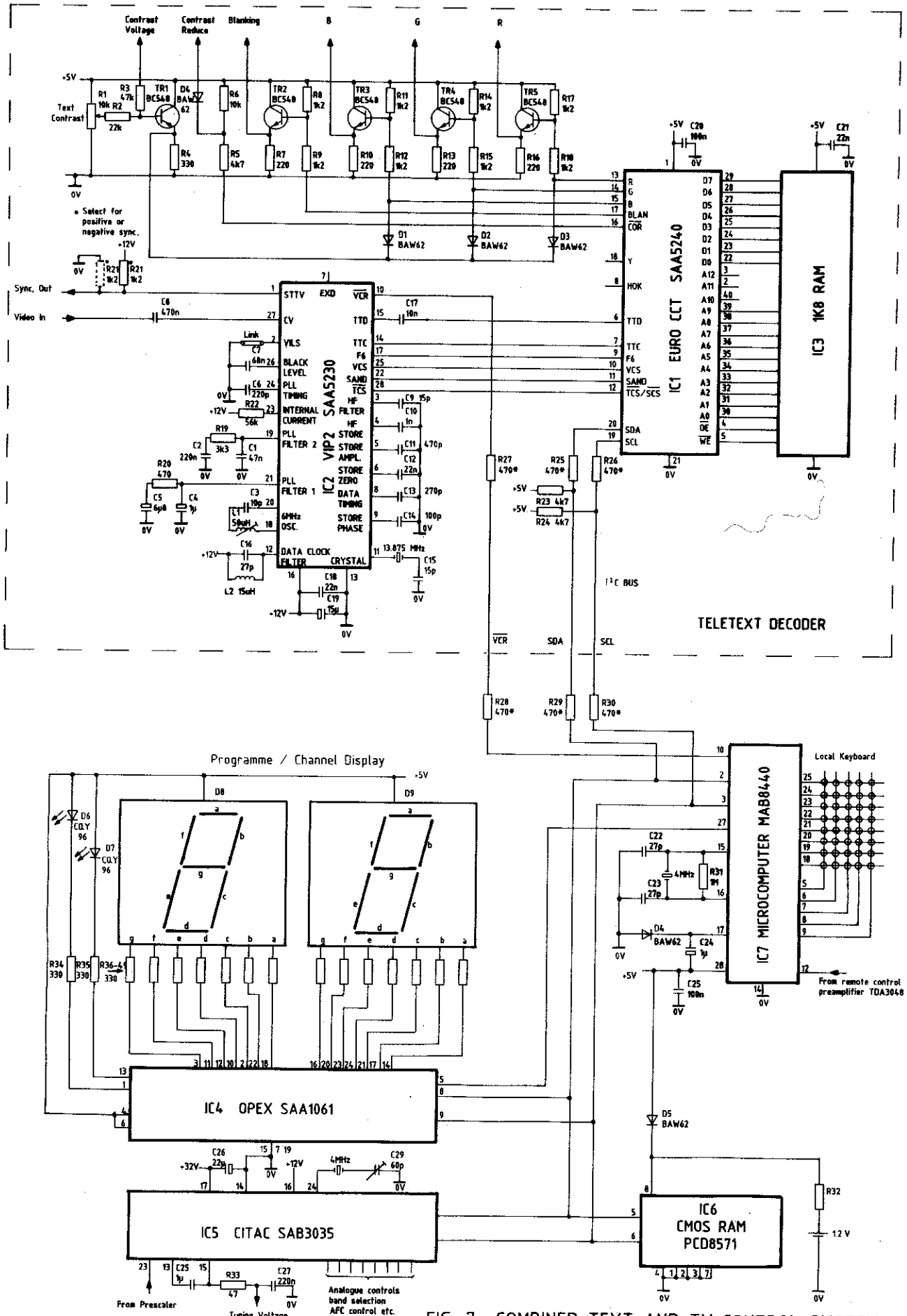


FIG. 7 COMBINED TEXT AND TV CONTROL SYSTEM

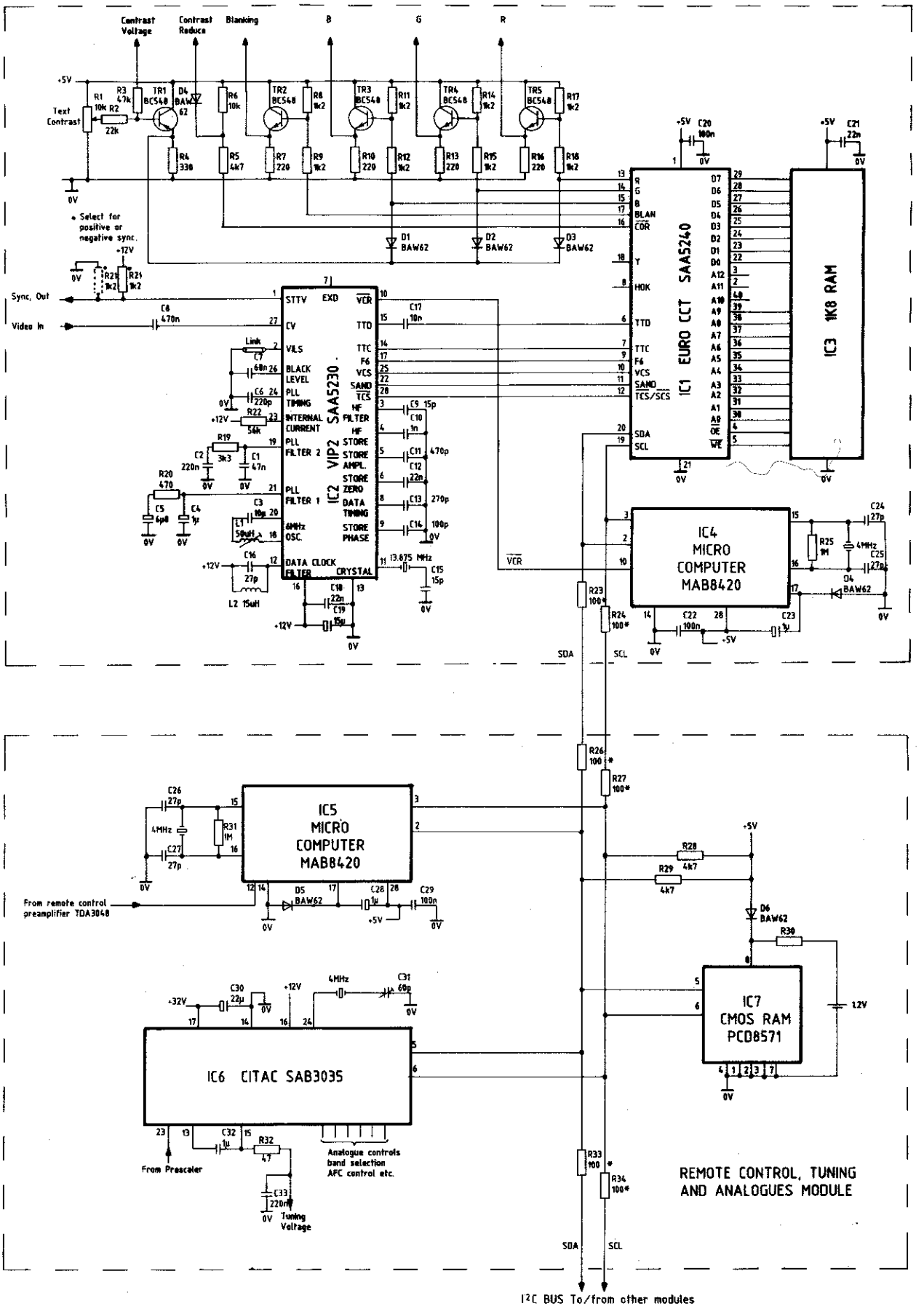


FIG. 8 MODULAR TEXT AND TV CONTROL SYSTEM

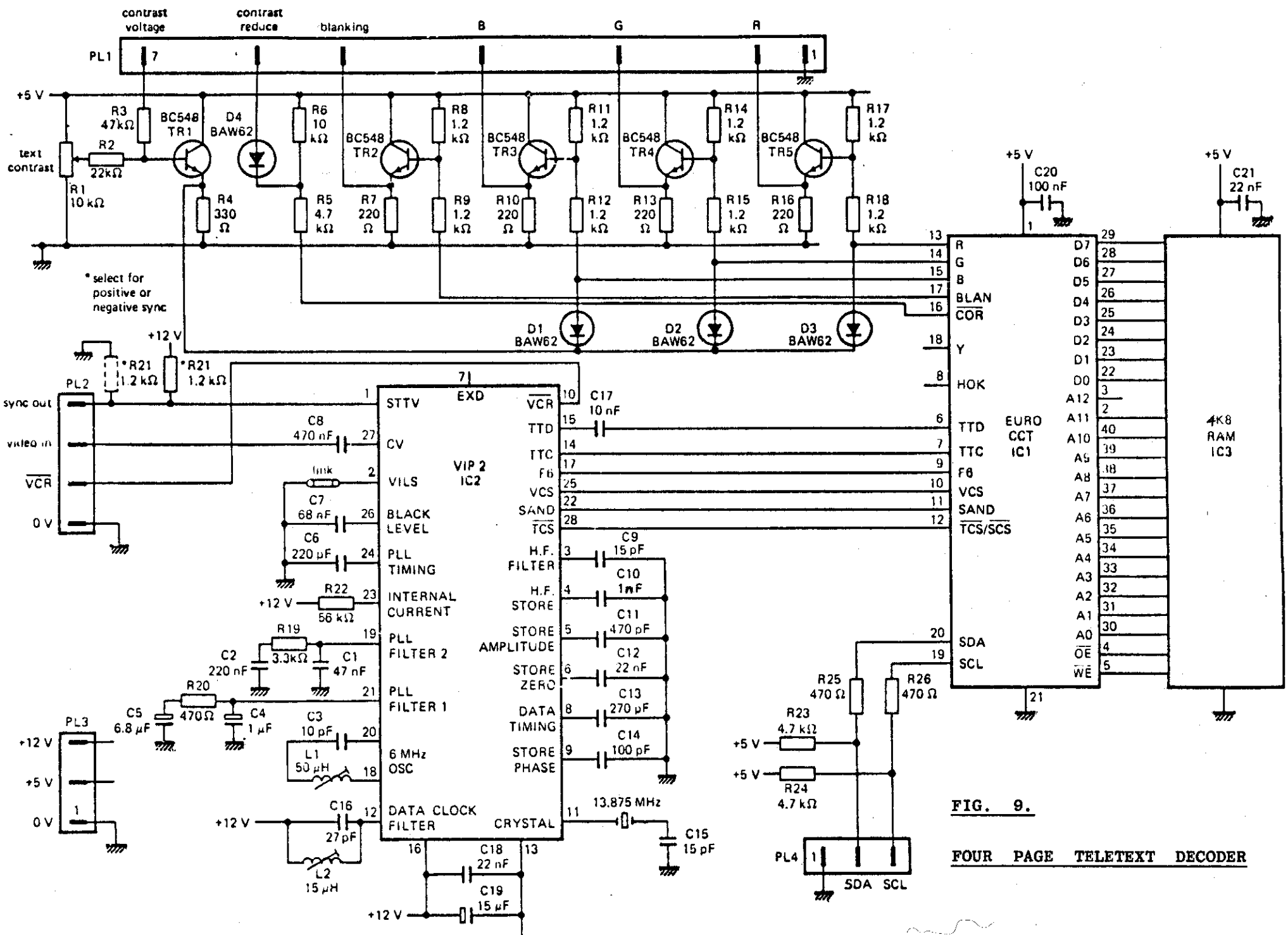


FIG. 9.

FOUR PAGE TELETEXT DECODER

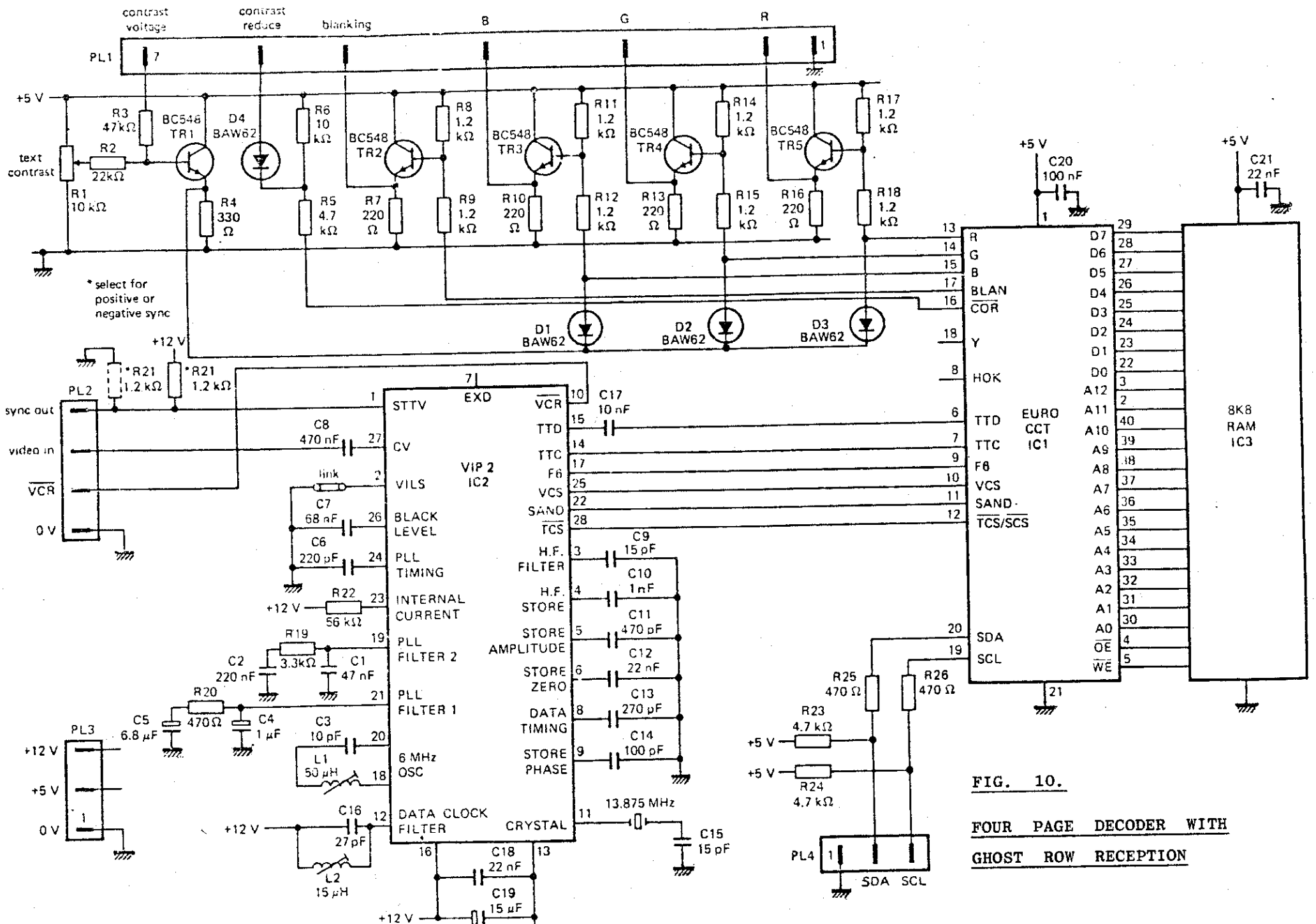


FIG. 10.

FOUR PAGE DECODER WITH GHOST ROW RECEPTION

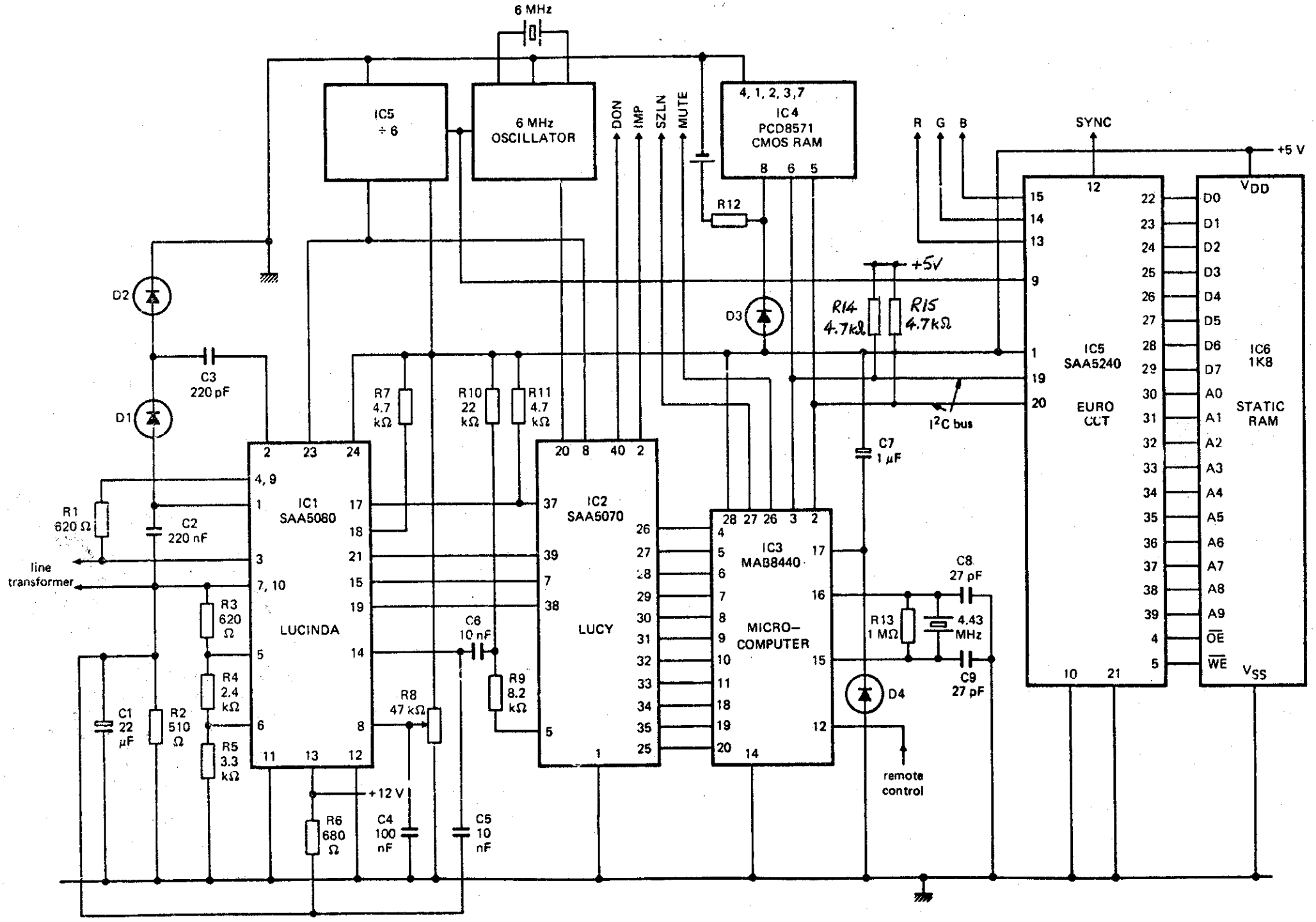


FIG. 11. VIEWDATA DECODER

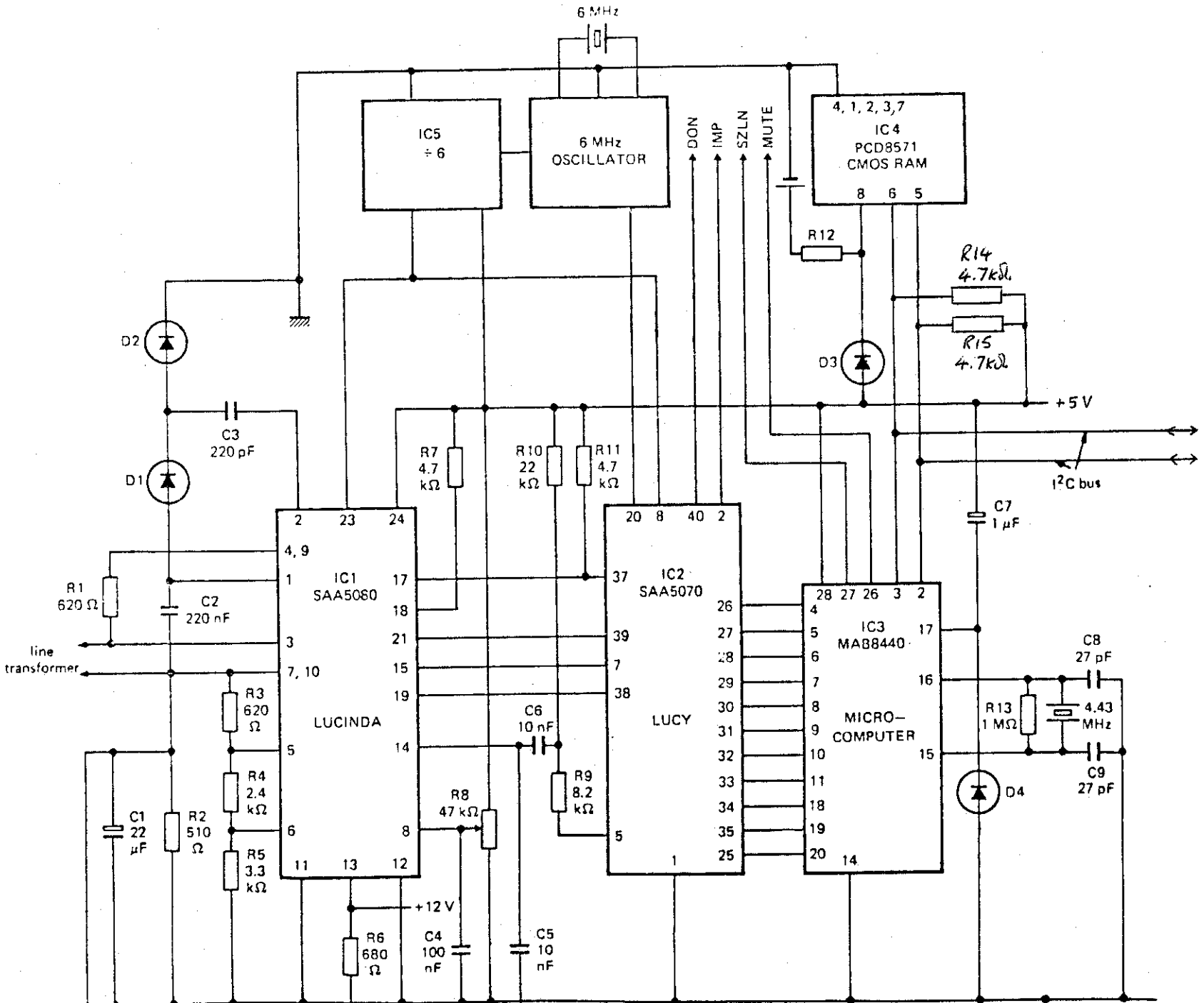


FIG. 12

VIEWDATA ADD-ON UNIT

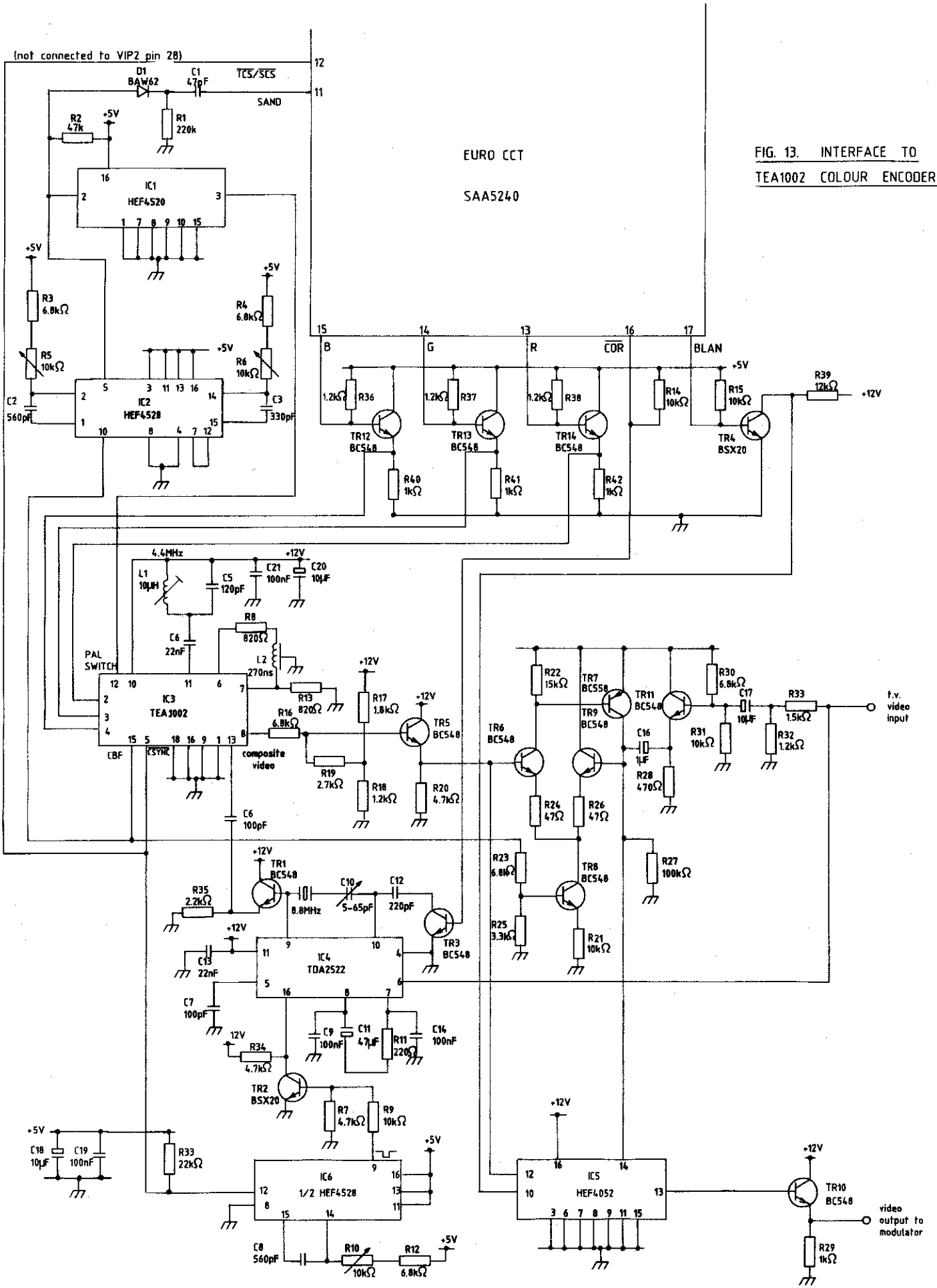


FIG. 13. INTERFACE TO TEA1002 COLOUR ENCODER

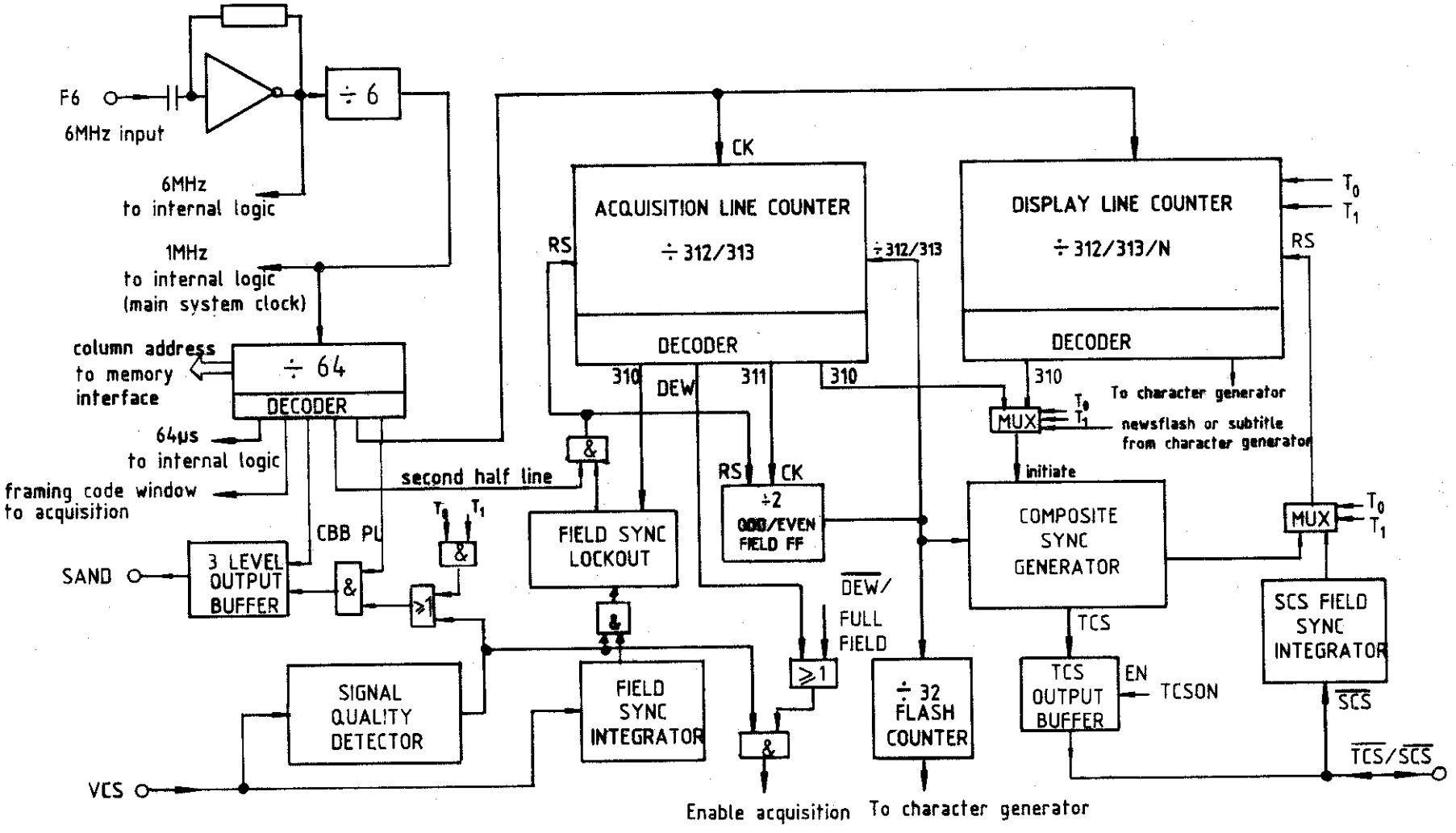
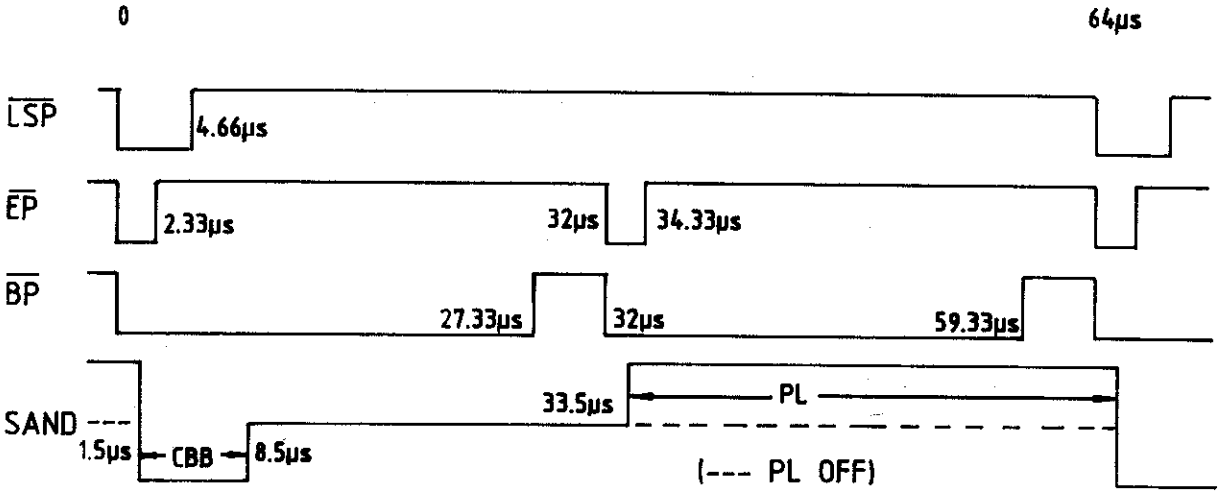
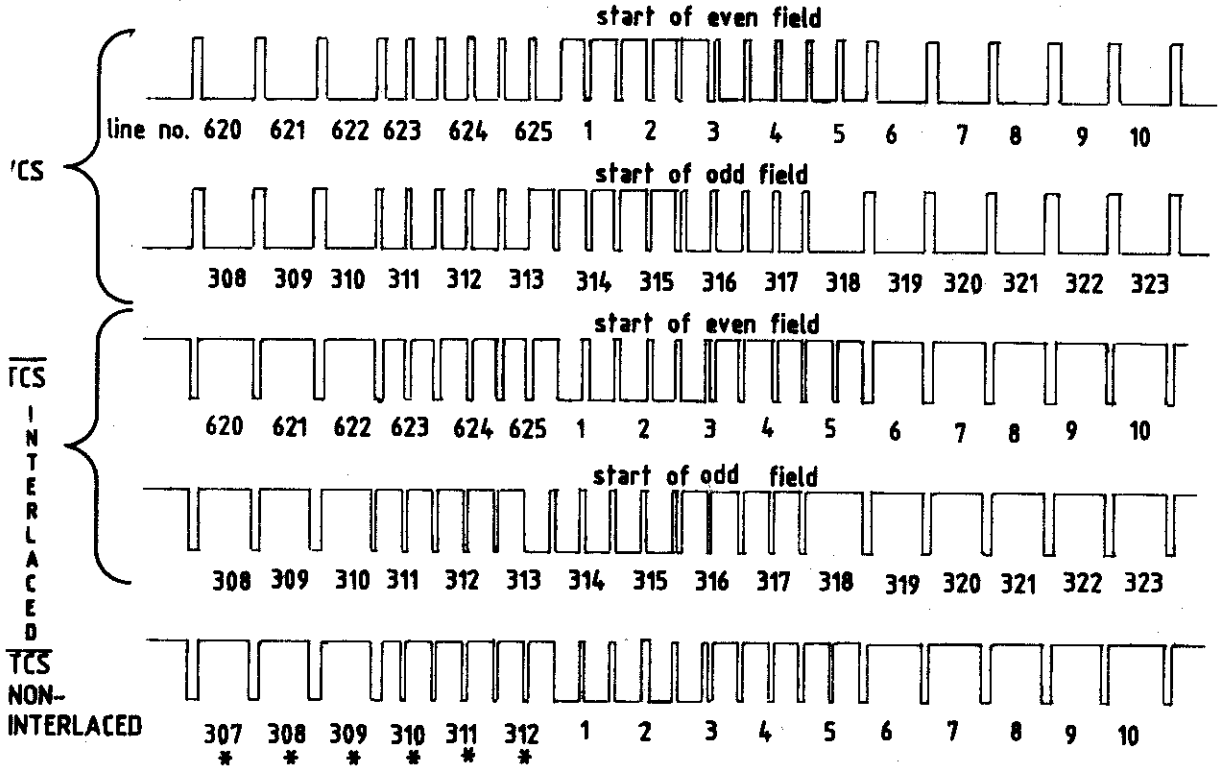


FIG. 14 TIMING CHAIN FUNCTION



$\overline{LSP}$, $\overline{EP}$ and $\overline{BP}$ are line sync., equalising and broad pulses combined to give $\overline{TCS}$ below

LINE RATE WAVEFORMS



* Add 1 to these numbers each alternate field for 312/313 line non-interlaced

FIG. 15 TIMING CHAIN WAVEFORMS

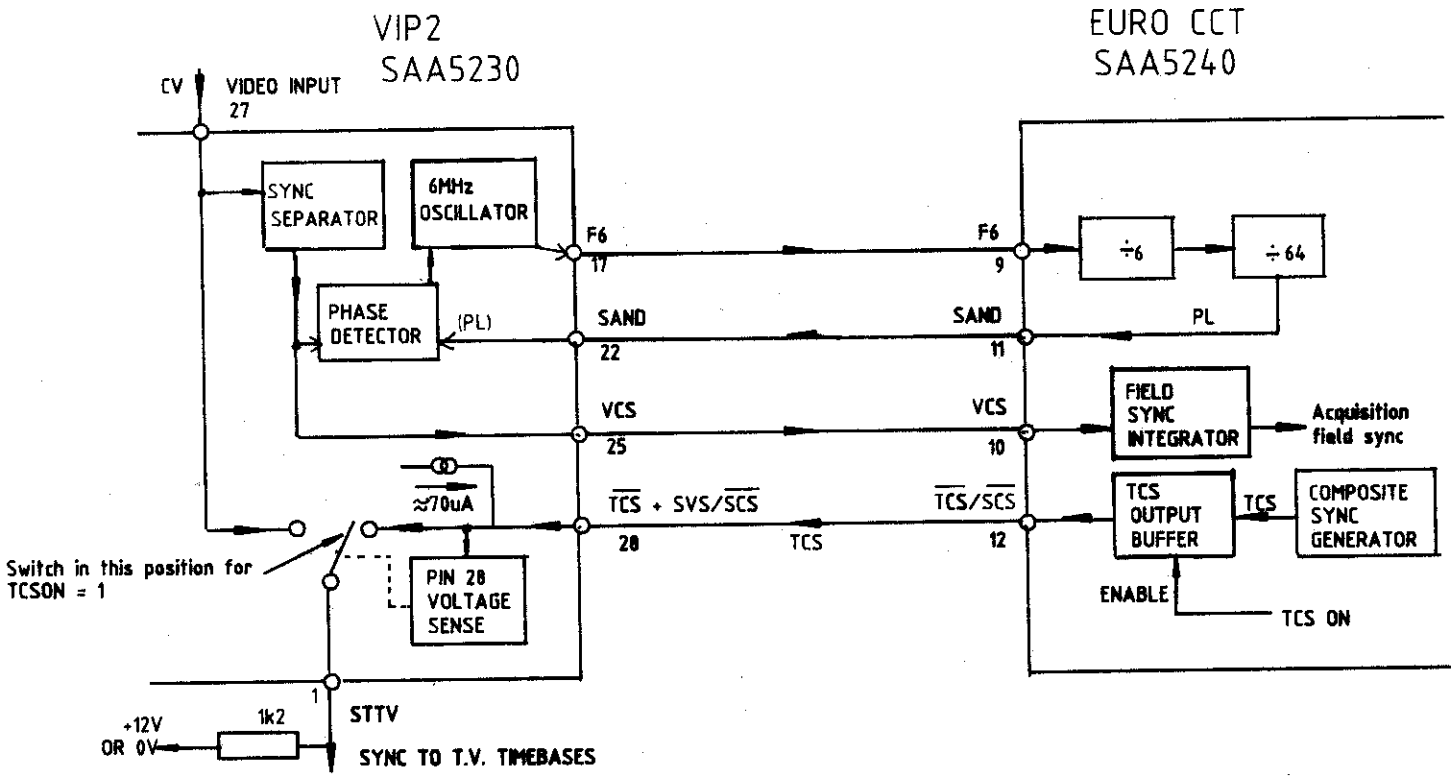


FIG. 16 NORMAL TIMING CONFIGURATION

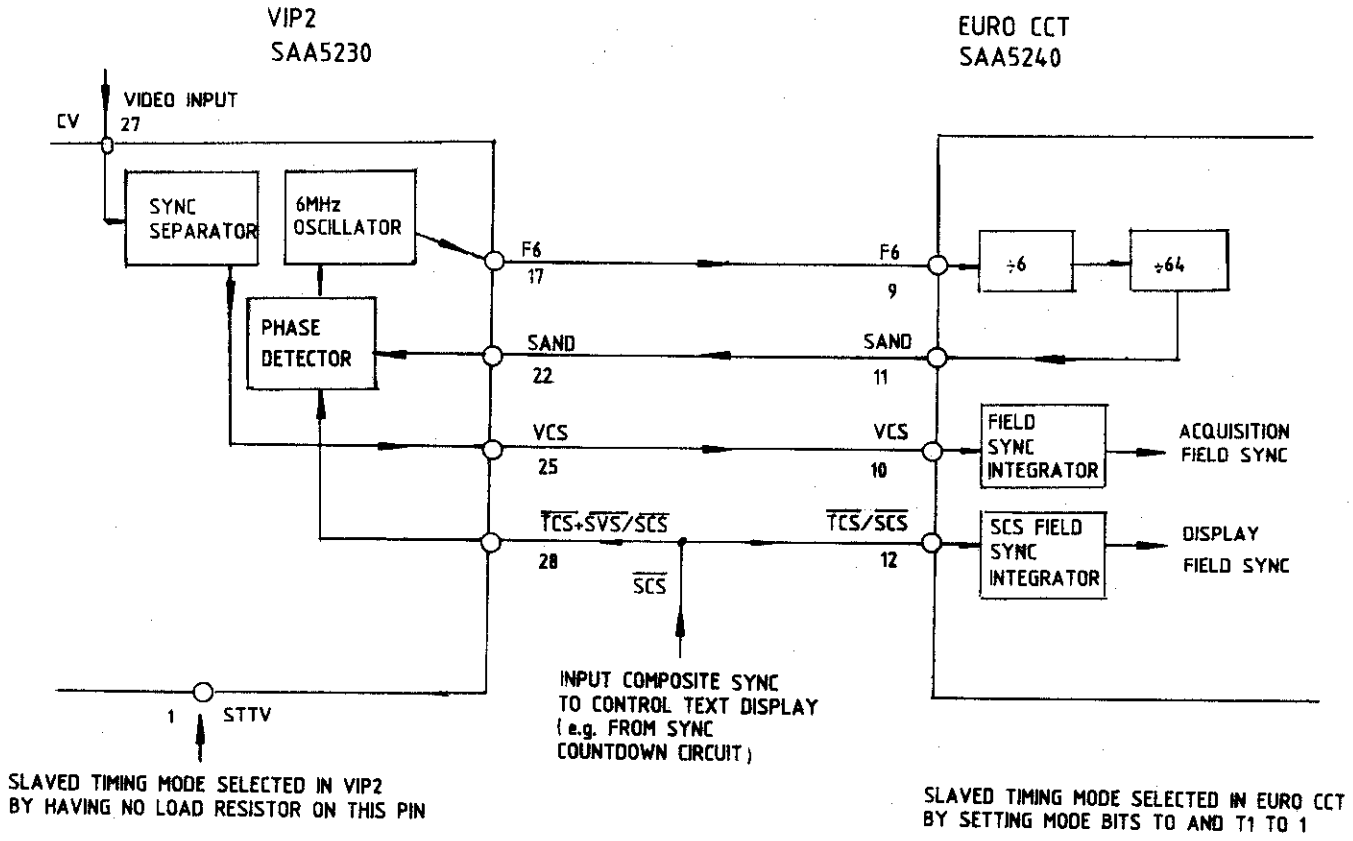


FIG. 17 SLAVED TIMING CONFIGURATION

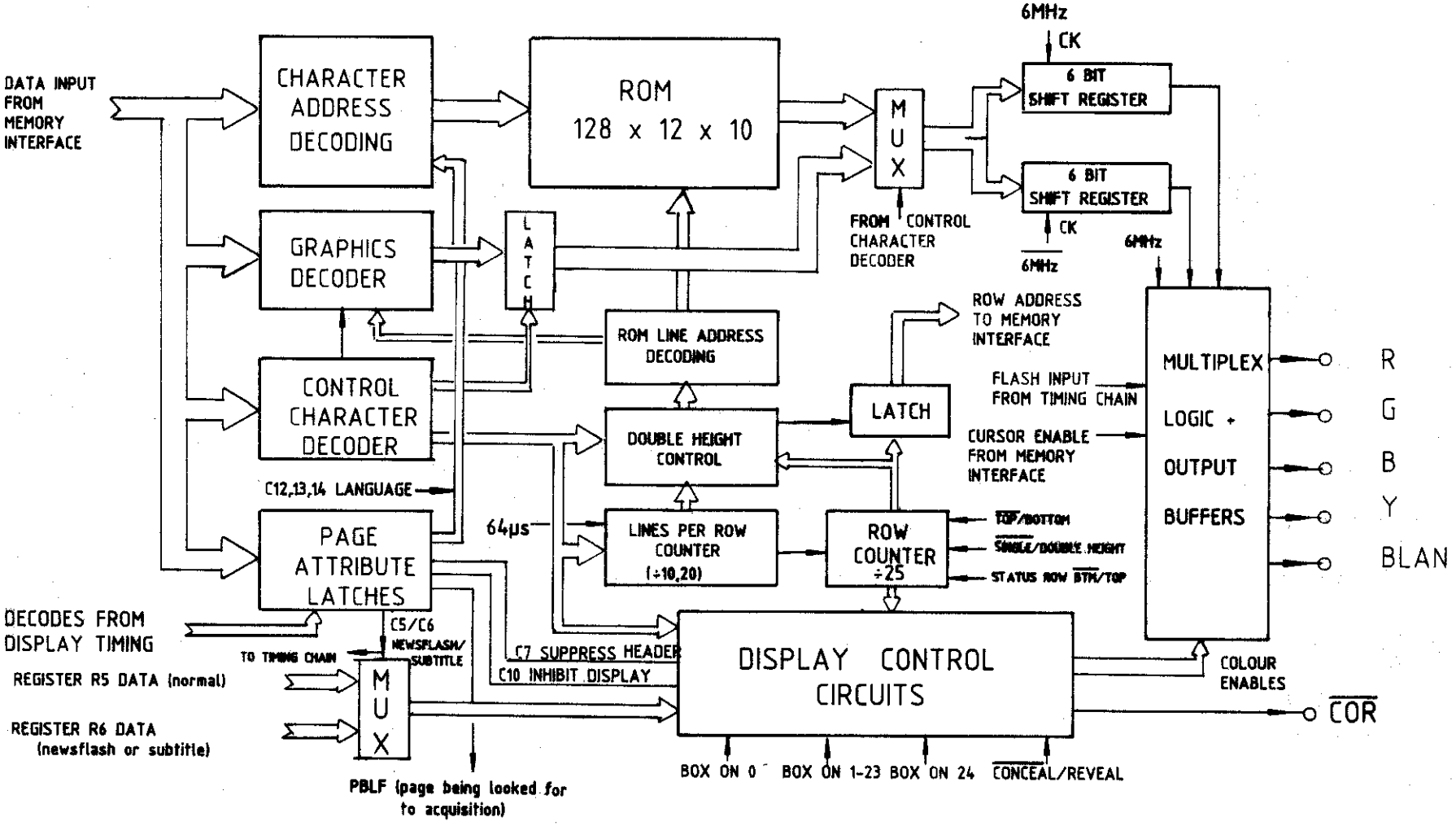


FIG. 18 CHARACTER GENERATOR FUNCTION

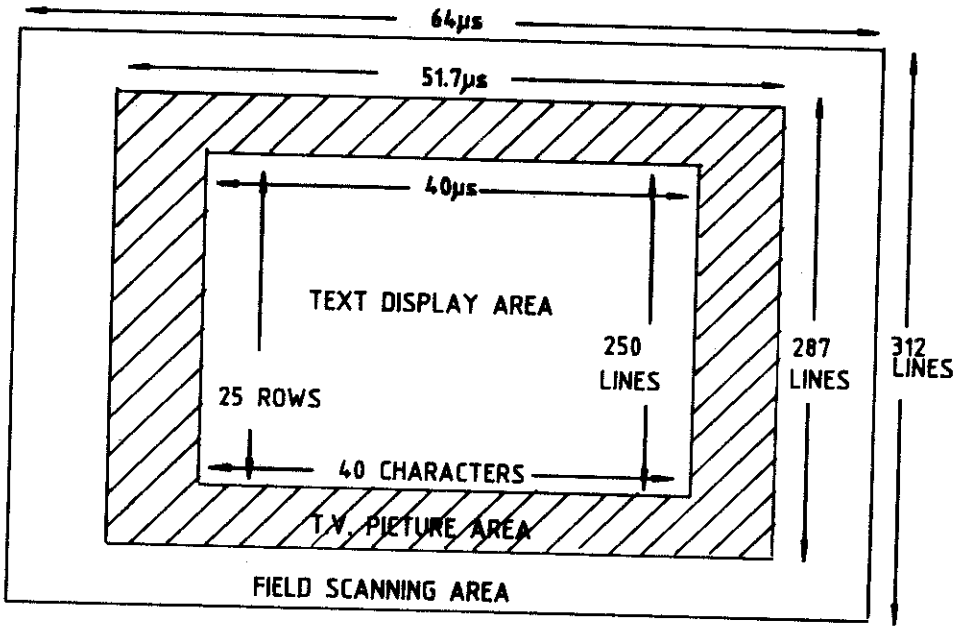


FIG. 19 DISPLAY FORMAT

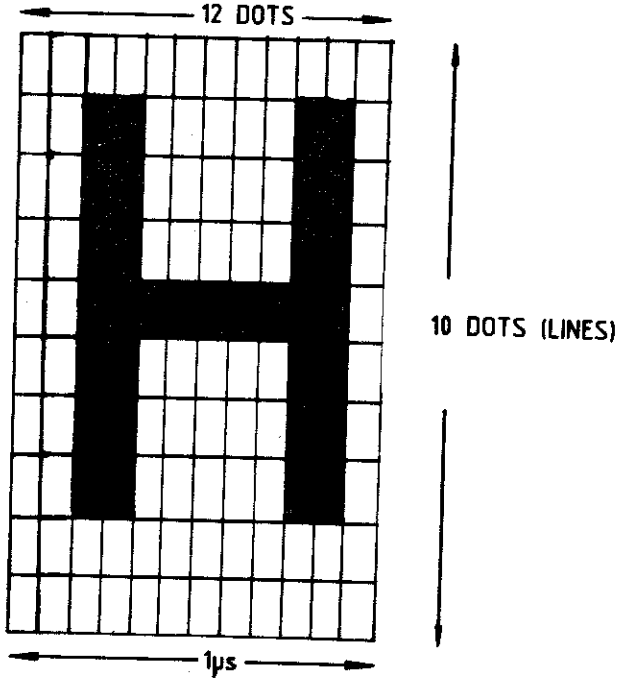


FIG. 20 CHARACTER MATRIX

b8=0

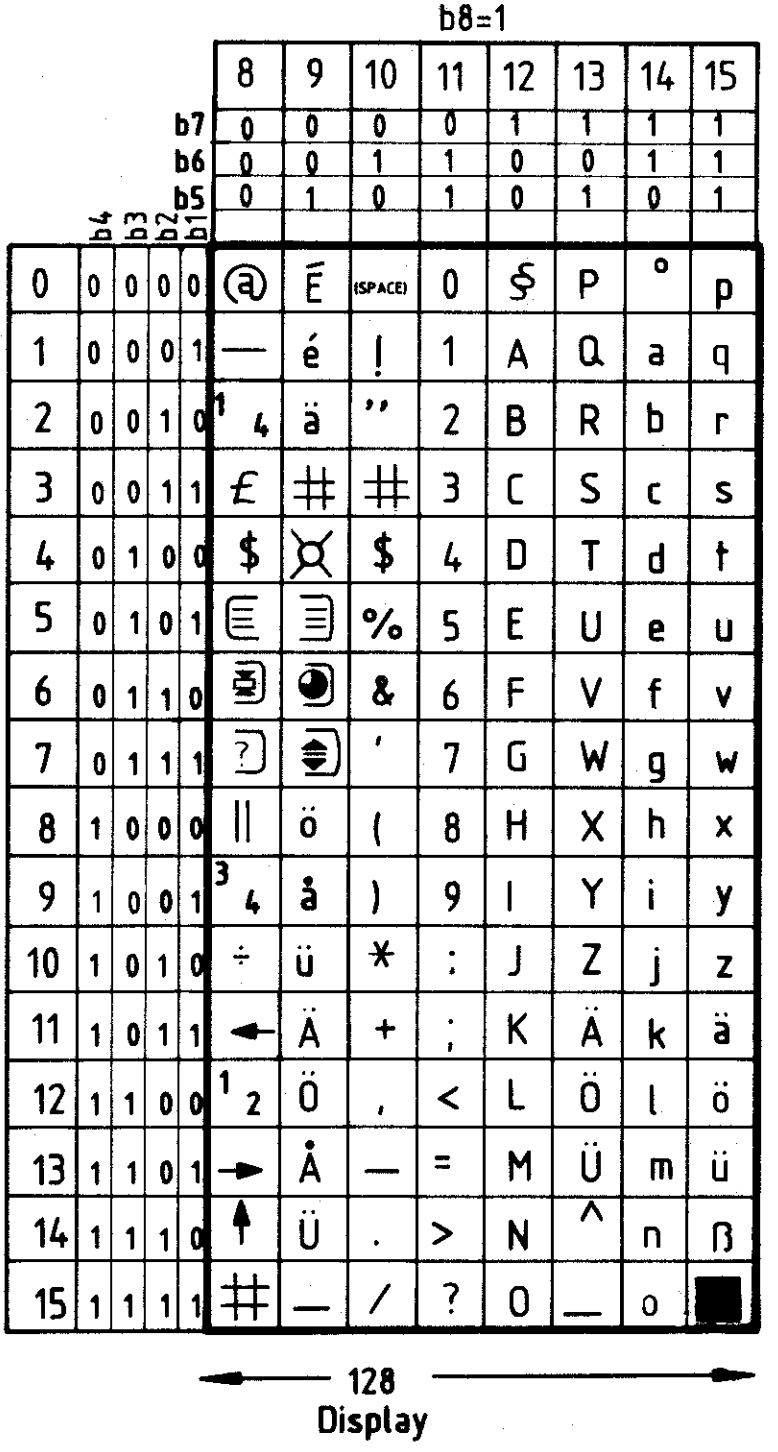
b4	b3	b2	b1	0 (b7=0, b6=0, b5=0)	1 (0,0,1)	2 (0,1,0)	3 (0,1,1)	4 (1,0,0)	5 (1,0,1)	6 (1,1,0)	7 (1,1,1)
0	0	0	0	α BLACK	γ BLACK	(SPACE)	0	@	P	—	p
1	0	0	0	1	α RED	γ RED	!	1	A	Q	a	q
2	0	0	1	0	α GREEN	γ GREEN	"	2	B	R	b	r
3	0	0	1	1	α YELLOW	γ YELLOW	£	3	C	S	c	s
4	0	1	0	0	α BLUE	γ BLUE	$	4	D	T	d	t
5	0	1	0	1	α MAGENTA	γ MAGENTA	%	5	E	U	e	u
6	0	1	1	0	α CYAN	γ CYAN	&	6	F	V	f	v
7	0	1	1	1	α WHITE	γ WHITE	'	7	G	W	g	w
8	1	0	0	0	FLASH	CONCEAL	(	8	H	X	h	x
9	1	0	0	1	STEADY	CONTIG γ	)	9	I	Y	i	y
10	1	0	1	0	END BOX	SEP γ	*	:	J	Z	j	z
11	1	0	1	1	START BOX	NO ACTION	+	;	K	←	k	¼
12	1	1	0	0	NORMAL HEIGHT	BLACK BK.GND	,	<	L	½	l	‖
13	1	1	0	1	DOUBLE HEIGHT	NEW BK.GND	-	=	M	→	m	¾
14	1	1	1	0	NO ACTION	HOLD γ	.	>	N	↑	n	÷
15	1	1	1	1	NO ACTION	RELEASE γ	/	?	O	#	o	■

32 Control — 96 Display

National Option Character Locations Shown :—

LANGUAGE	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü

FIG. 21 NATIONAL OPTION CHARACTER SET (BIT 8 = 0)



The symbols in rows 5, 6 and 7 columns 8 and 9 are intended for use in pairs as status indicators. Their meaning is as follows:-

Text Page hold Time Reveal

Size

FIG. 22. FIXED CHARACTER SET WITH BIT 8=1

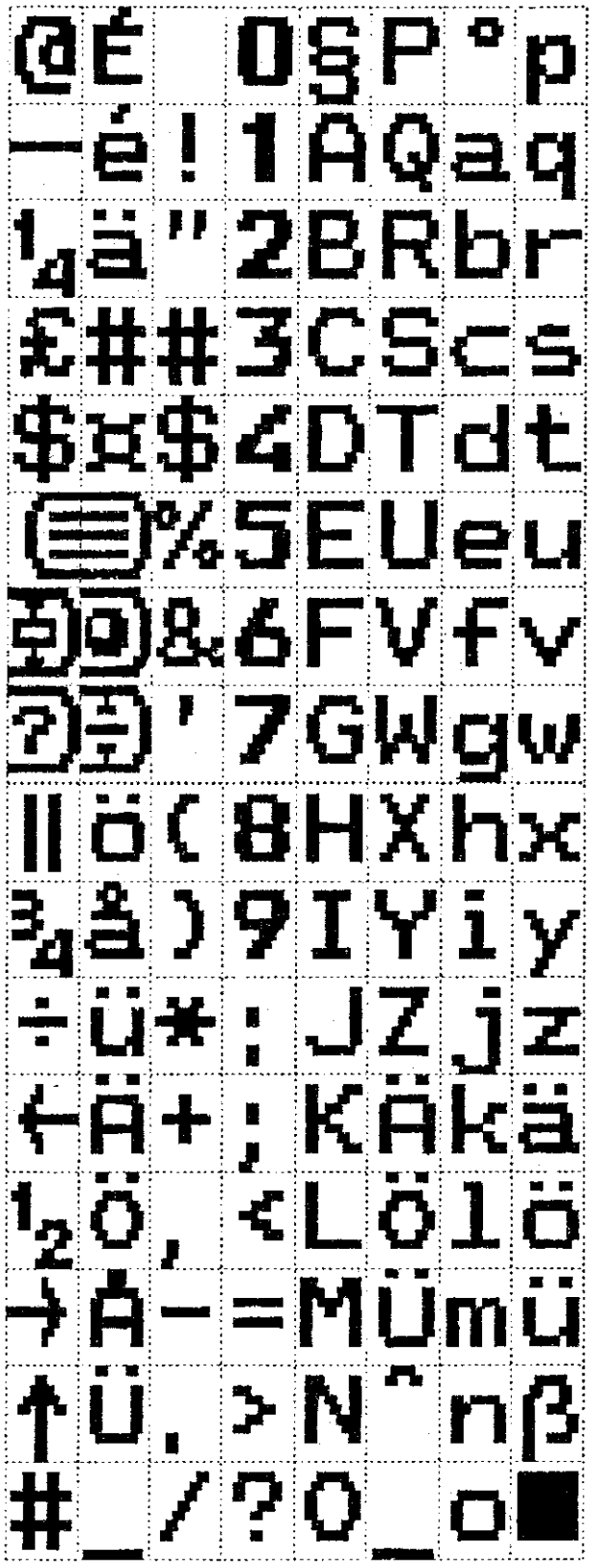


FIG. 23. CHARACTER SET DOT MATRIX PATTERNS

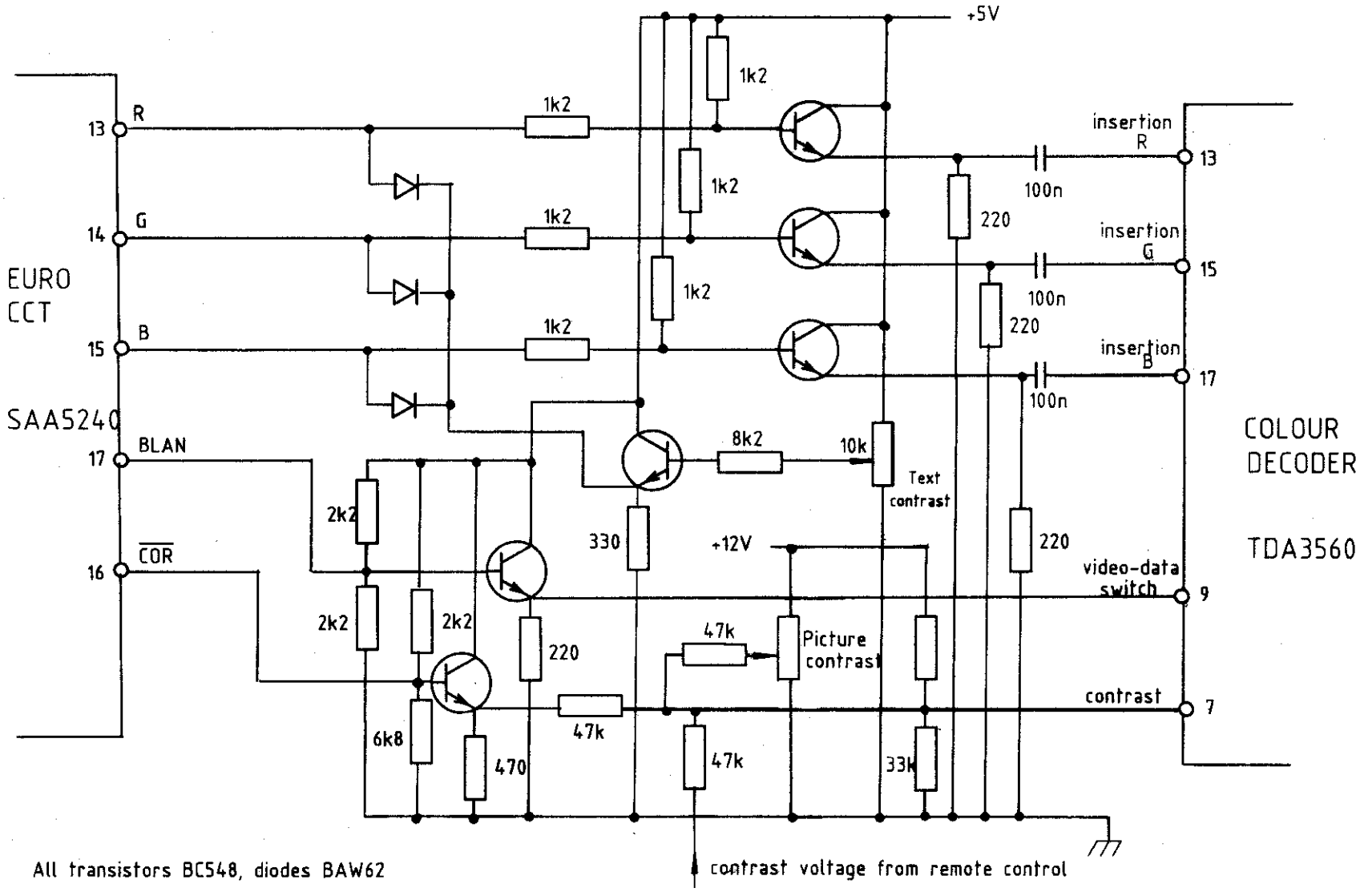
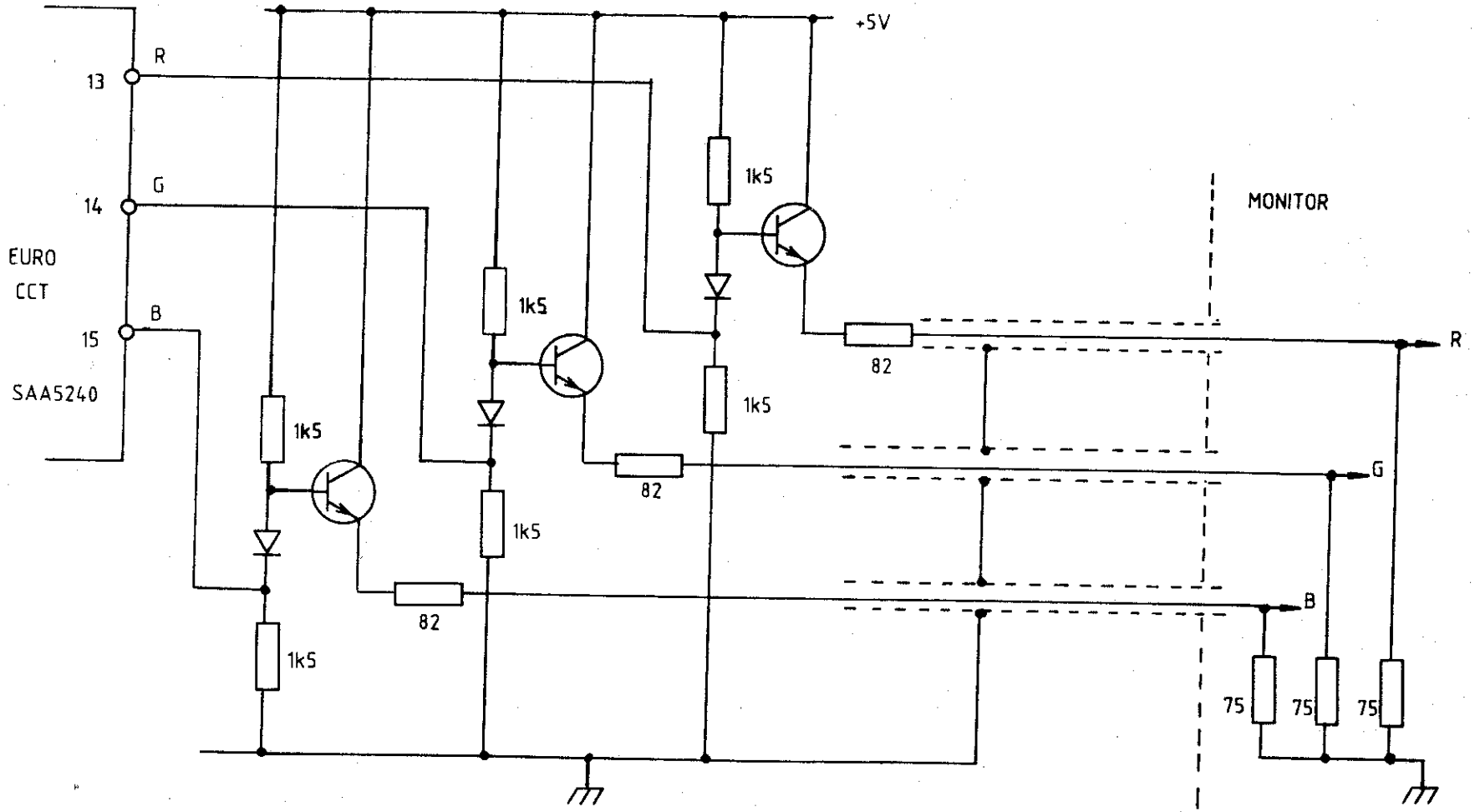


FIG. 24. OUTPUT INTERFACE TO TDA3560 CIRCUIT



All transistors BC548, diodes BAW62.

FIG. 25 OUTPUT INTERFACE FOR TEXT MONITOR

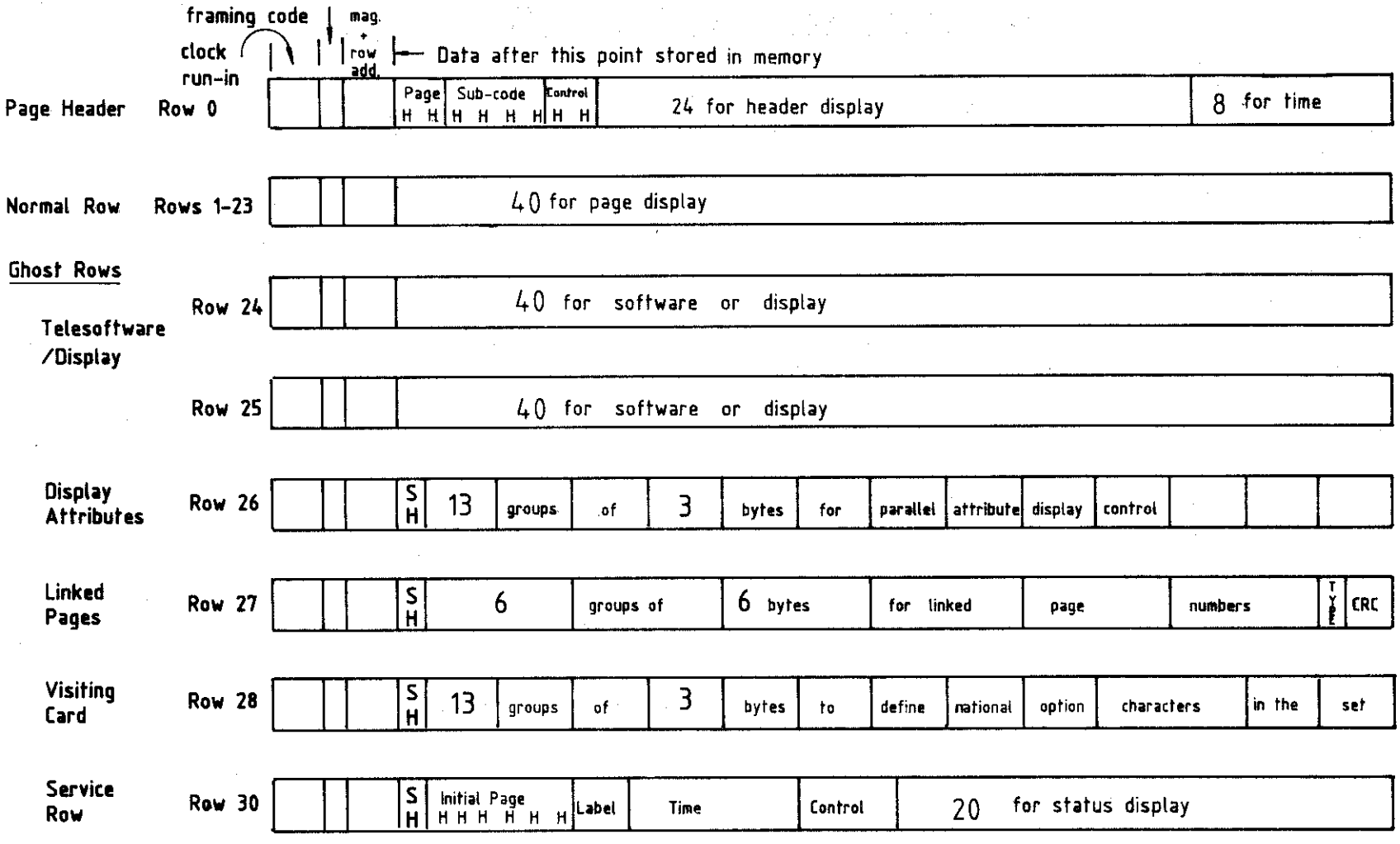


FIG. 26 TELETEXT ROWS RECEIVED BY EURO CCT

COLUMN	D7	D6	D5	D4	D3	D2	D1	D0
0	X	X	X	Do Care Mag.	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	X	X	X	Do Care Page Tens	PT3	PT2	PT1	PT0
2	X	X	X	Do Care Page Units	PU3	PU2	PU1	PU0
3	X	X	X	Do Care Hours Tens	X	X	HT1	HT0
4	X	X	X	Do Care Hours Units	HU3	HU2	HU1	HU0
5	X	X	X	Do Care Minutes Tens	X	MT2	MT1	MT0
6	X	X	X	Do Care Minutes Units	MU3	MU2	MU1	MU0

X = DON'T CARE MAG = MAGAZINE PT = PAGE TENS

PU = PAGE UNITS HT = HOURS TENS HU = HOURS UNITS

MT = MINUTES TENS MU = MINUTES UNITS

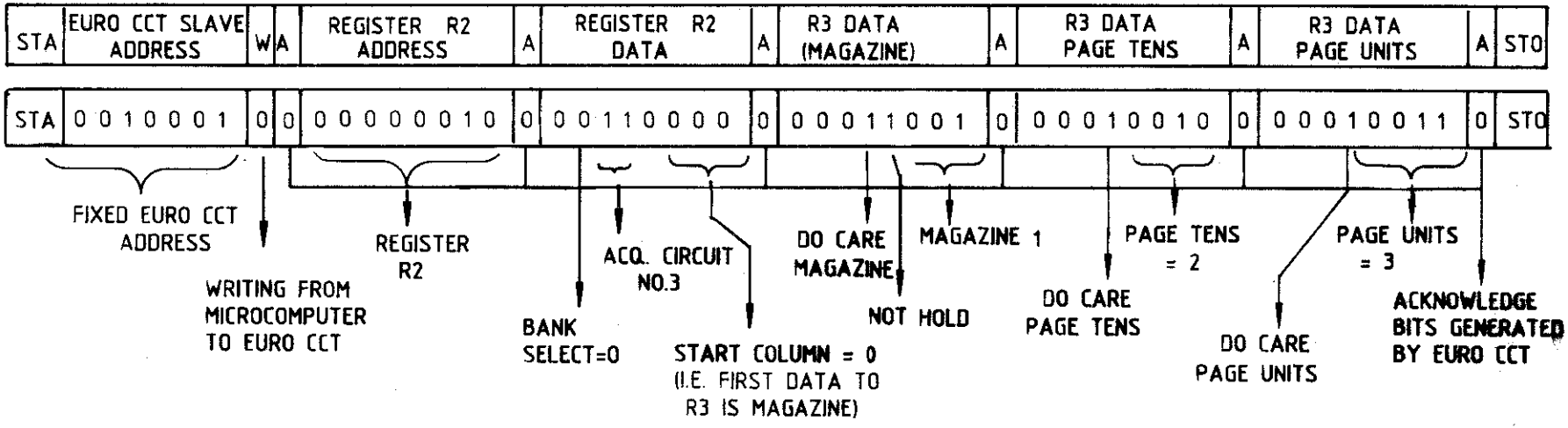
ALL DATA WRITTEN TO REGISTER R3, WITH COLUMN NUMBER DEFINED BY PREVIOUS DATA IN REGISTER R2 (AUTO-INCREMENTS).

FIG. 27 PAGE REQUEST DATA FORMAT

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R_2	—	BANK SELECT A2	ACQ. CIRCUIT A1	ACQ. CIRCUIT A0	T_B	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0

Auto increments to R3

Bit D3 (T_B) is for test purposes and must be 0 for normal operation



EXAMPLE I^2C TRANSMISSION: REQUESTING PAGE 123 IN ACQUISITION CIRCUIT NO.3 FOR MEMORY NO.3
(ASSUMES SUB-CODE DIGITS WERE NOT USED OR ARE UNALTERED)

FIG. 28 REGISTER R2 ORGANISATION AND EXAMPLE OF PAGE REQUEST SEQUENCE

COLUMN	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Hamming Error PU	PU3	PU2	PU1	PU0
1	0	0	0	Hamming Error PT	PT3	PT2	PT1	PT0
2	0	0	0	Hamming Error MU	MU3	MU2	MU1	MU0
3	0	0	0	Hamming Error MT	C4	MT2	MT1	MT0
4	0	0	0	Hamming Error HU	HU3	HU2	HU1	HU0
5	0	0	0	Hamming Error HT	C6	C5	HT1	HT0
6	0	0	0	Hamming Error CTRL A	C10	C9	C8	C7
7	0	0	0	Hamming Error CTRL B	C14	C13	C12	C11
8	0	0	0	$\overline{\text{FOUND}}$	0	MAG2	MAG1	MAG0
9	0	0	PBLF	0	0	0	0	0

PU = PAGE UNITS PT = PAGE TENS MU = MINUTES UNITS

MT = MINUTES TENS HU = HOURS UNITS HT = HOURS TENS

C4 = ERASE C5 = NEWSFLASH C6 = SUBTITLE

C7 = SUPPRESS HEADER C8 = UPDATE C9 = INTERRUPTED SEQUENCE

C10 = INHIBIT DISPLAY C11= MAGAZINE SERIAL C12,13,14 = LANGUAGE SELECTION

FIG. 29 ROW 25 DATA FORMAT

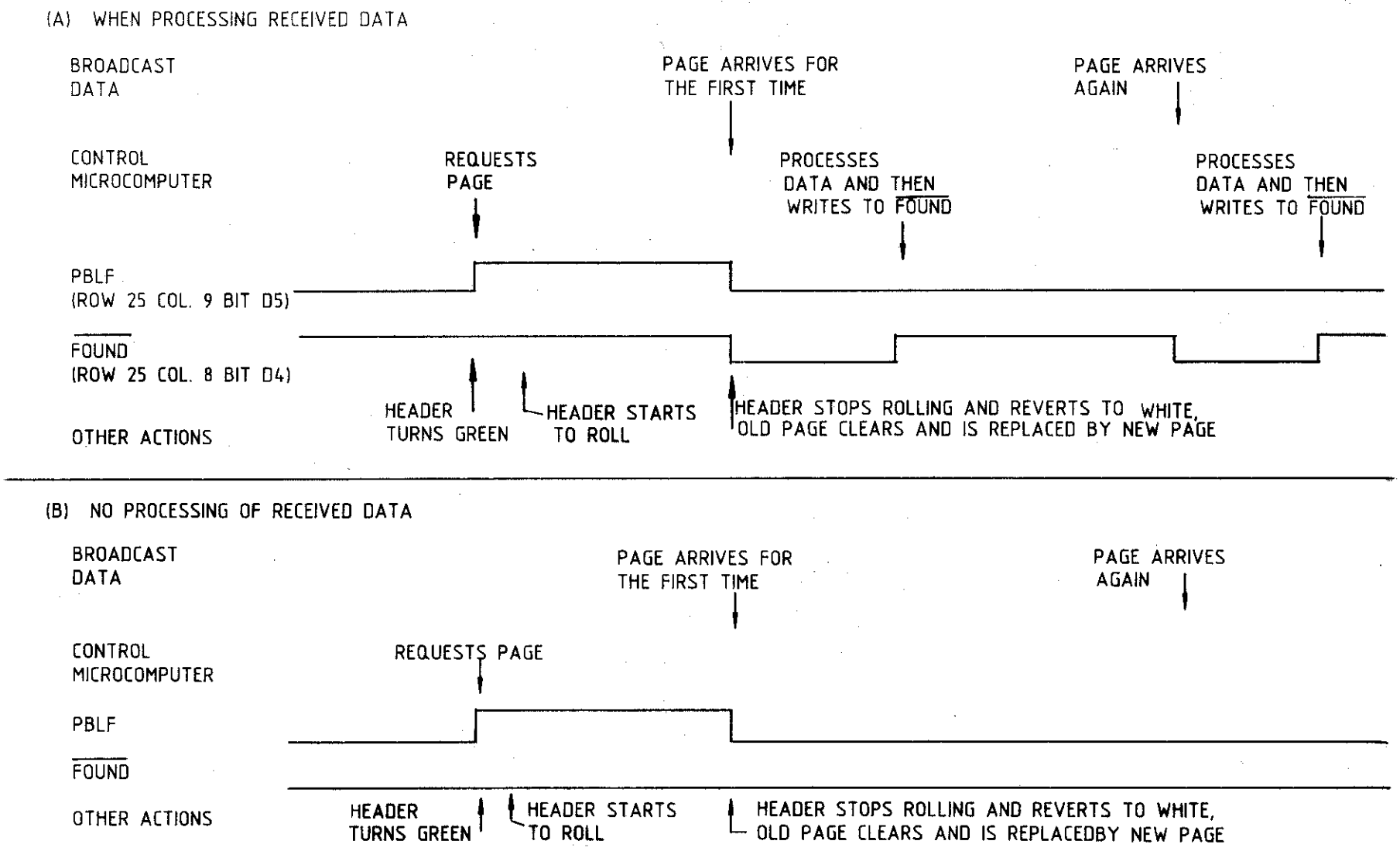


FIG. 30 OPERATION OF THE PBLF AND $\overline{\text{FOUND}}$ BITS

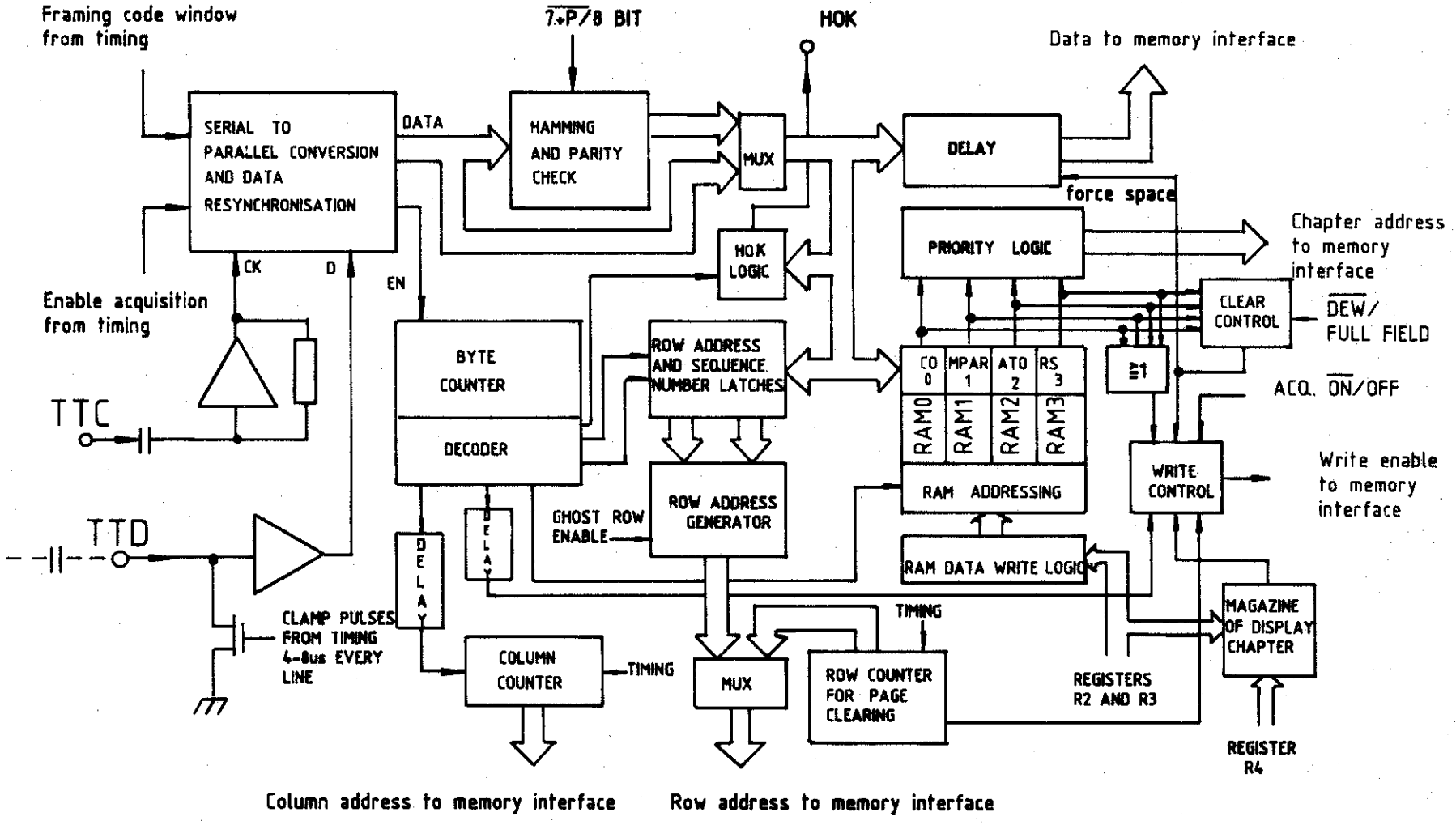


FIG. 31. ACQUISITION SECTION BLOCK DIAGRAM

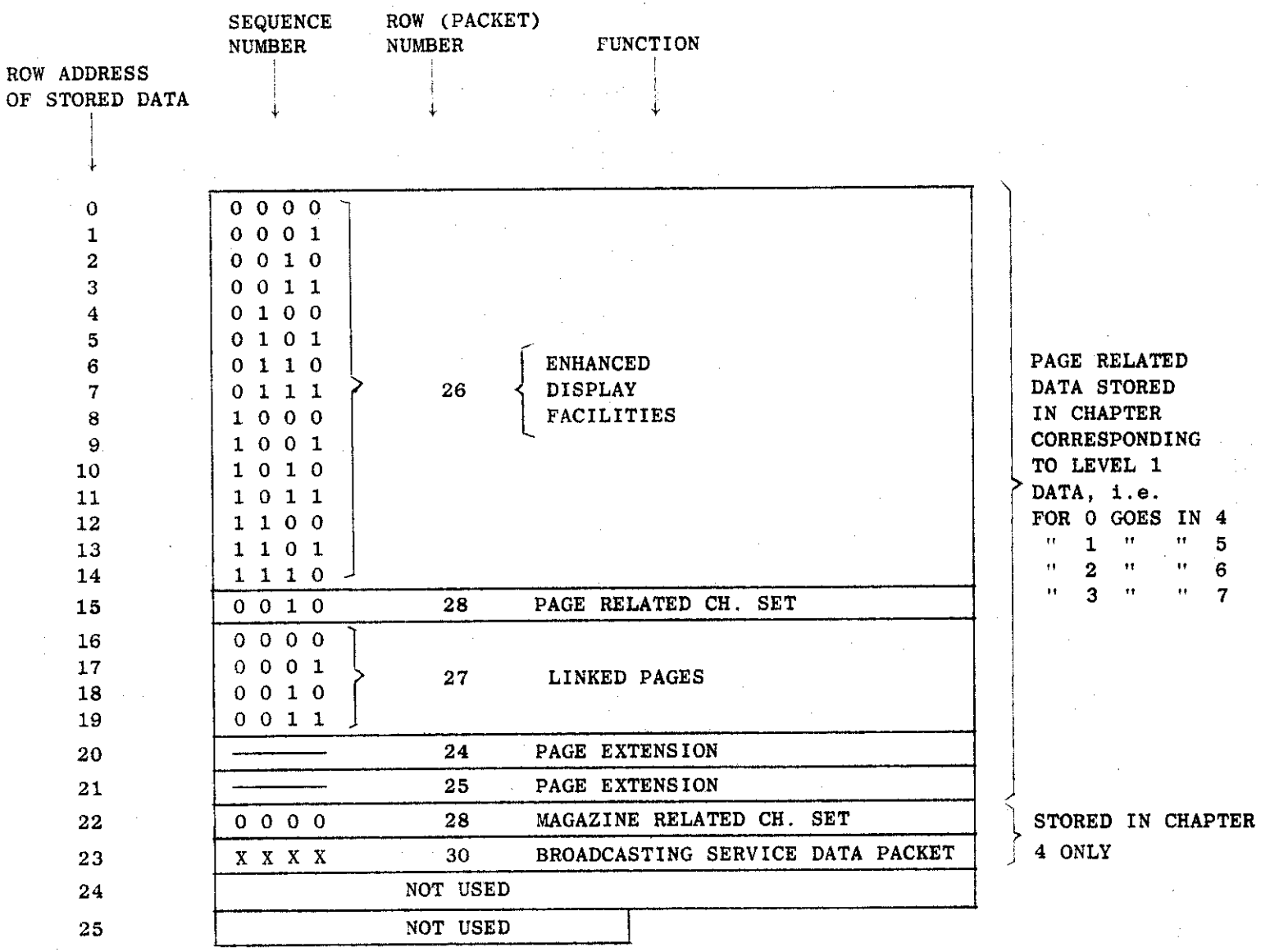


FIG. 32 - GHOST ROW ADDRESS MAPPING

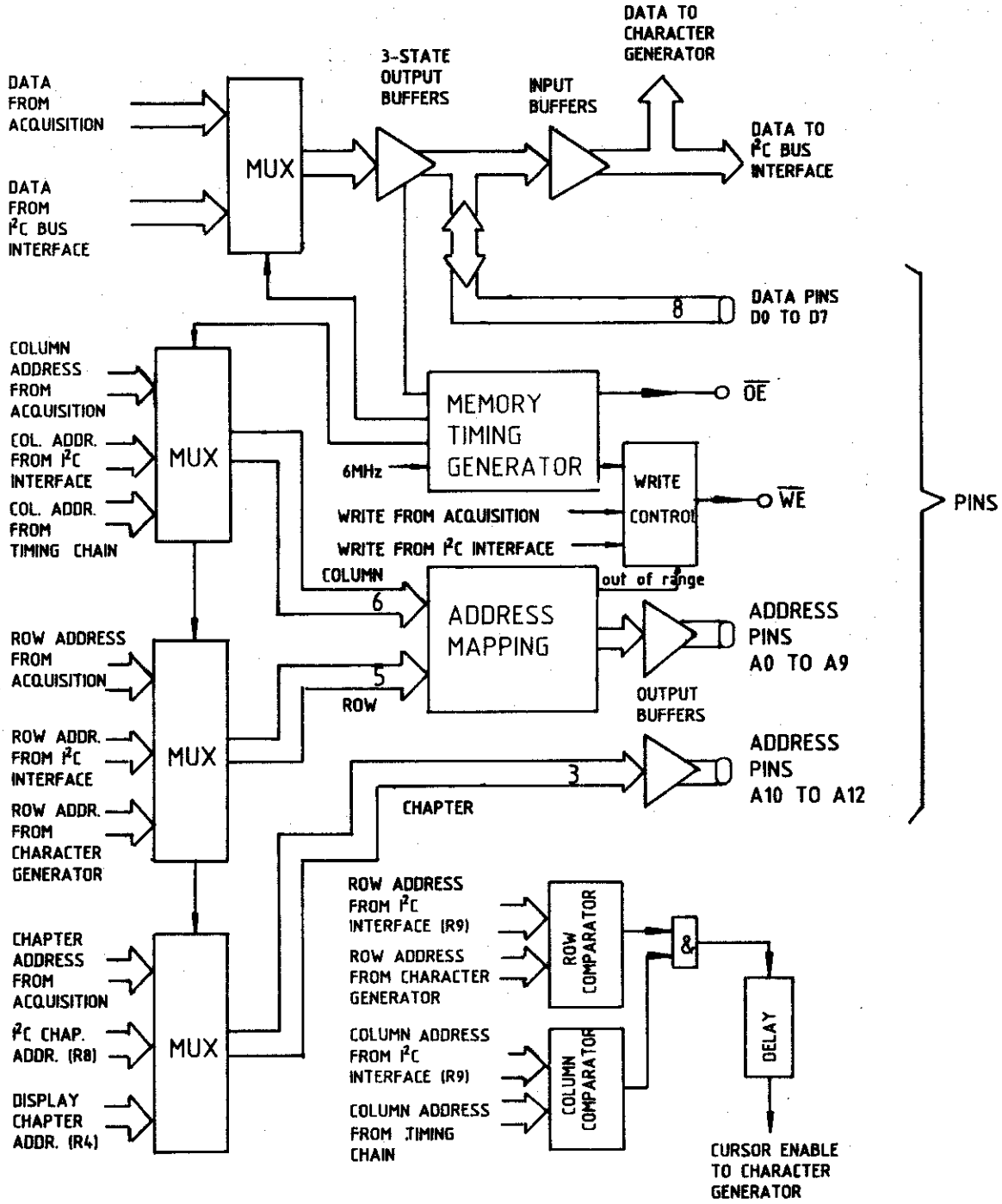


FIG. 33 MEMORY INTERFACE

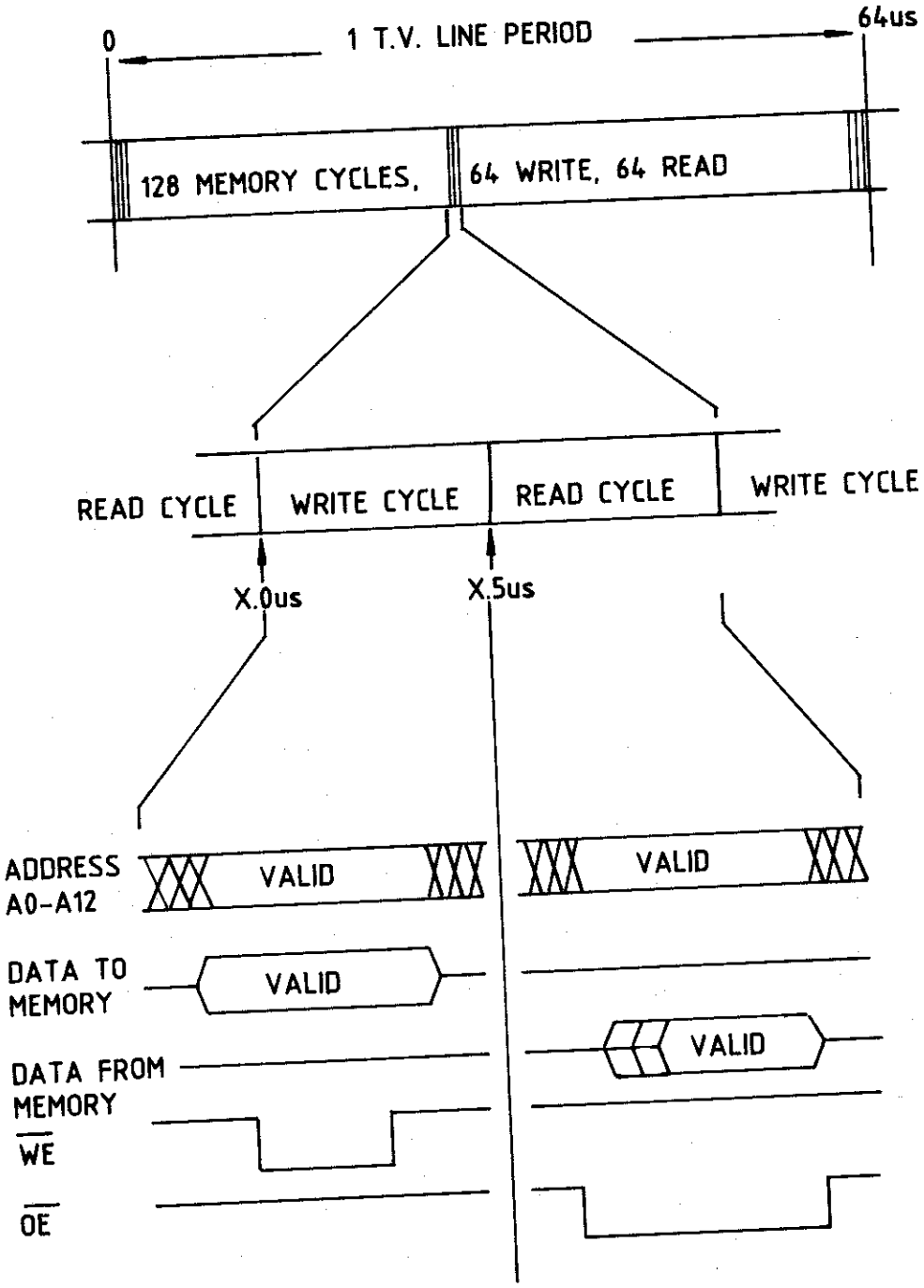


FIG. 34 MEMORY CYCLES

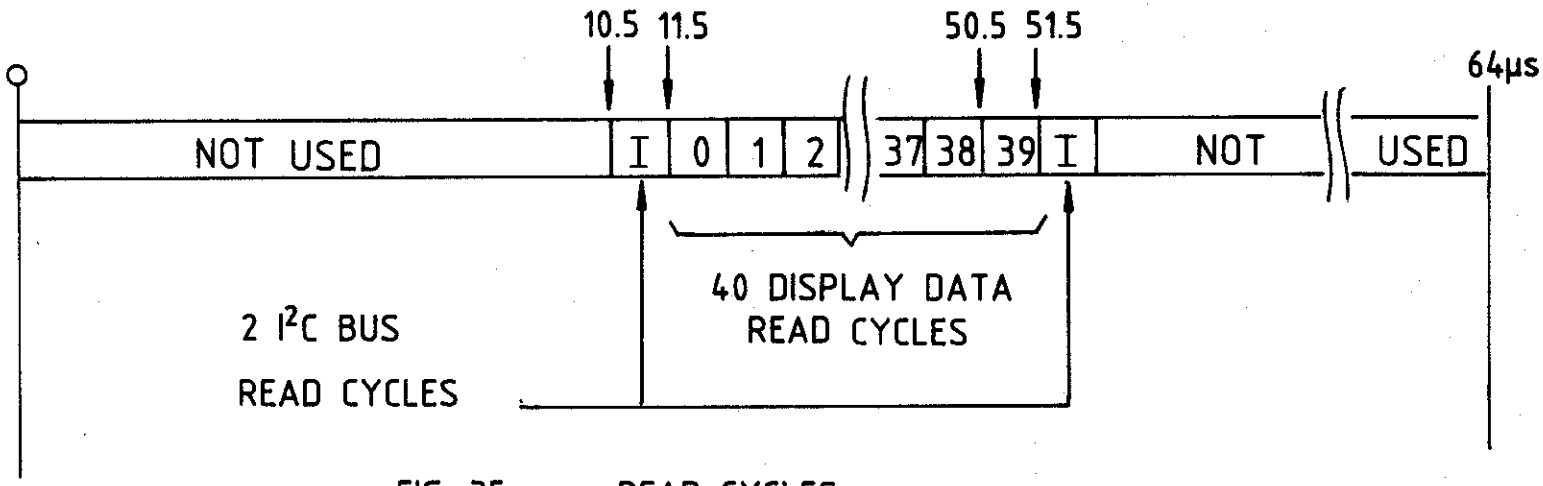


FIG. 35 READ CYCLES

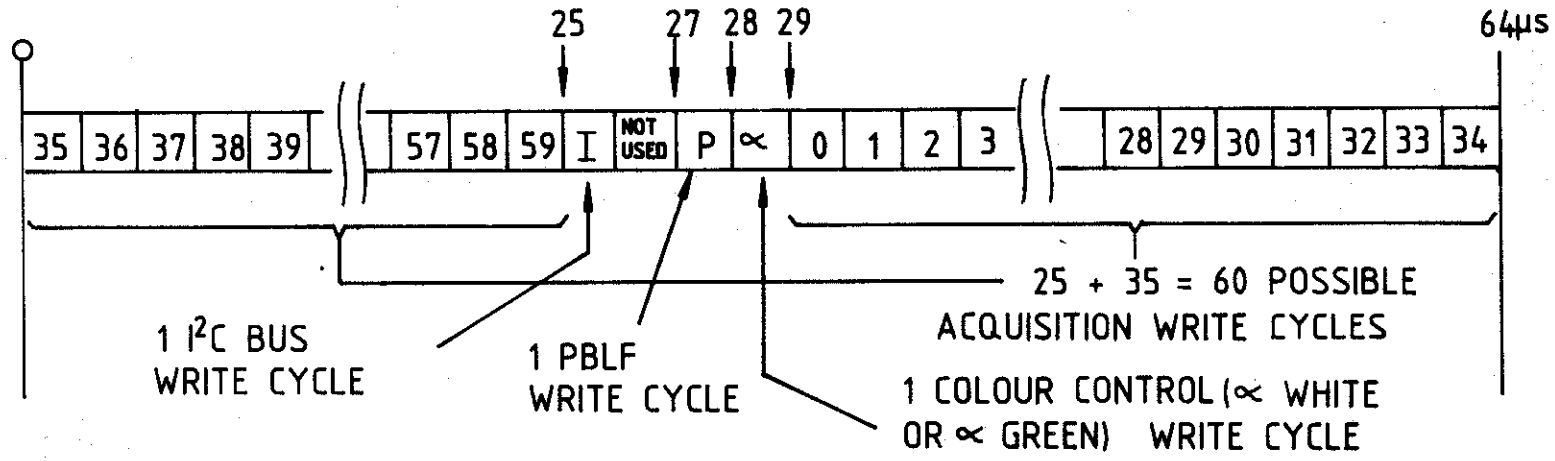


FIG. 36 WRITE CYCLES

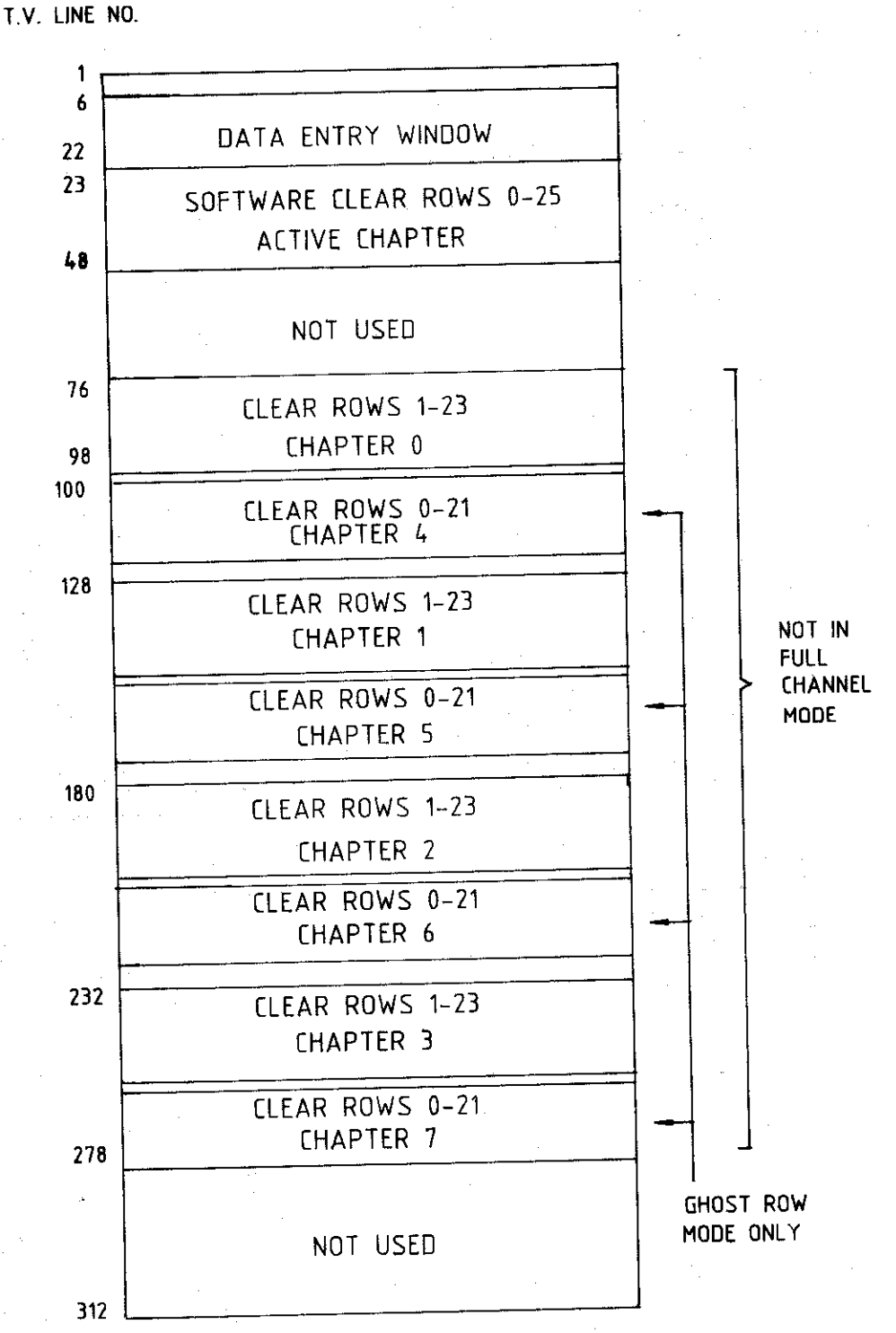
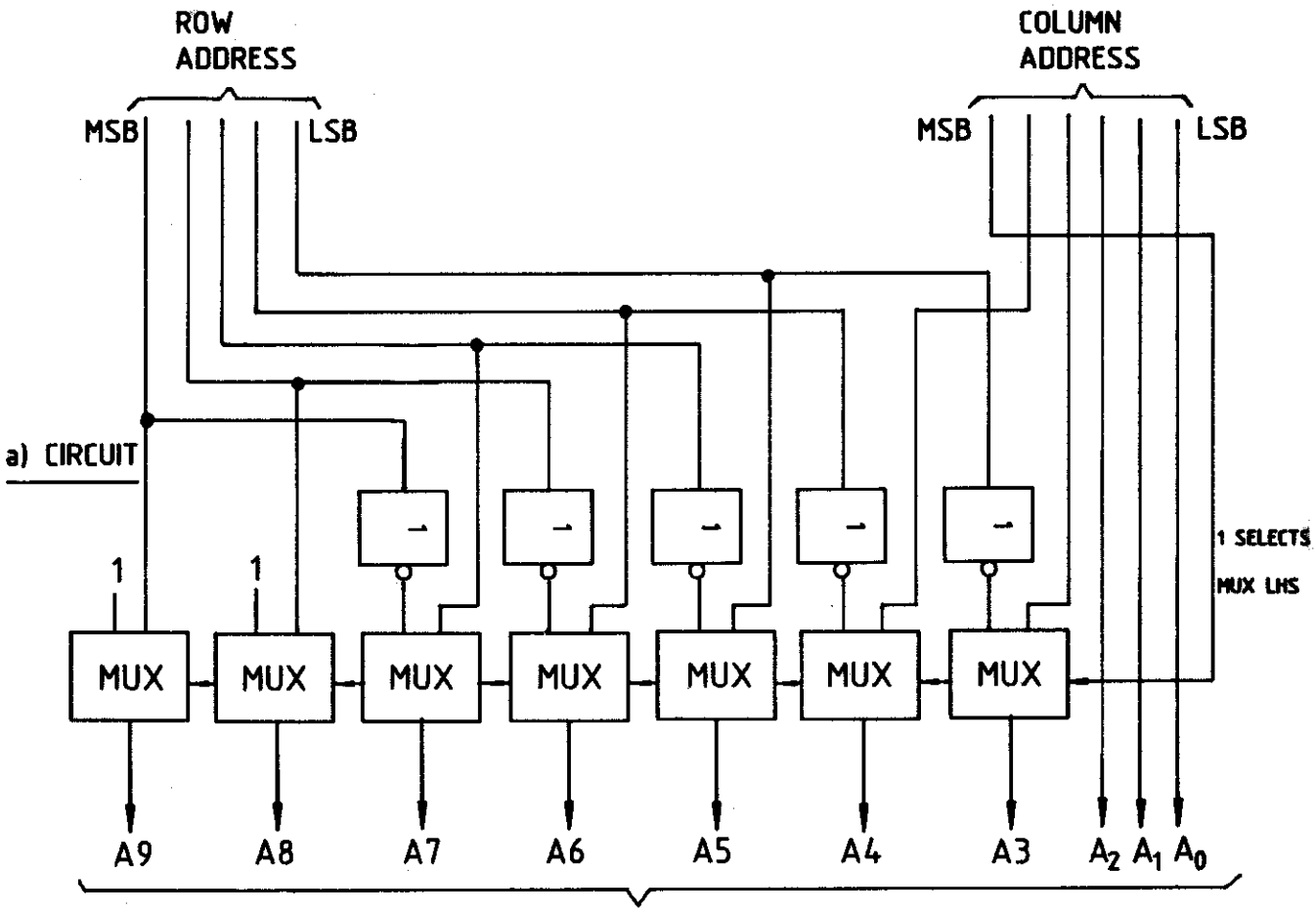


FIG. 37 WRITE CYCLE ALLOCATION PER FIELD



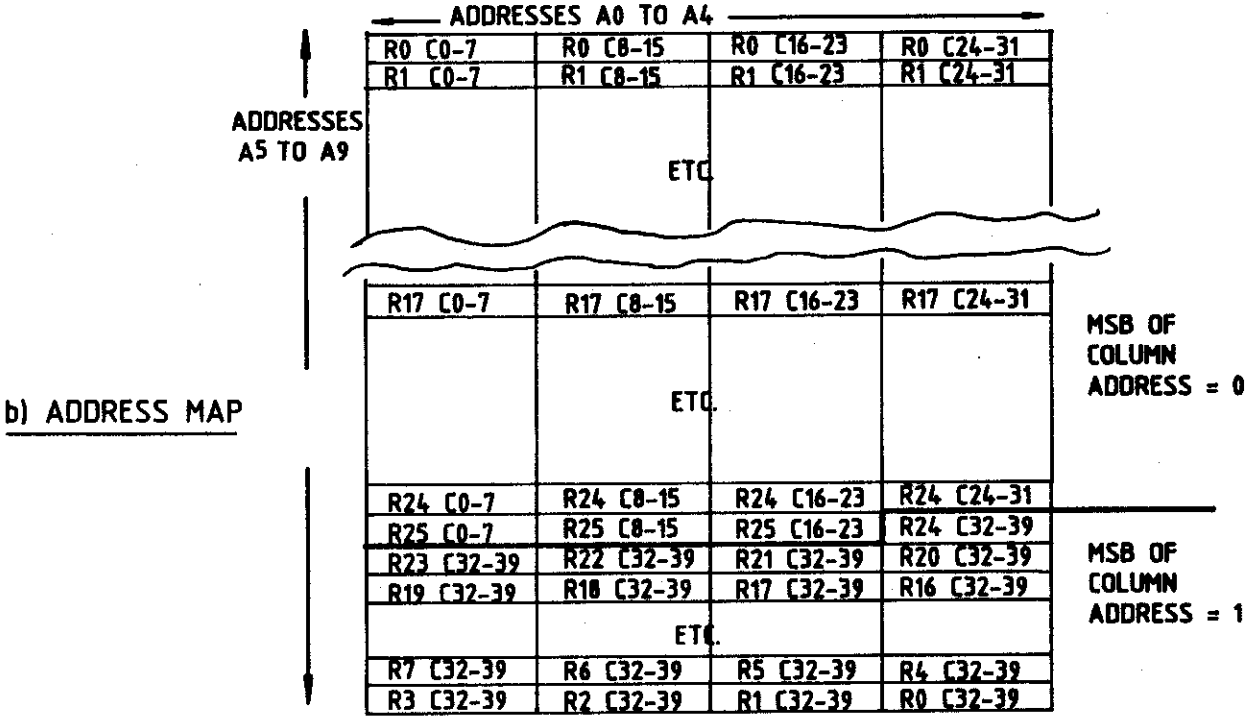


FIG. 38 ADDRESS MAPPING

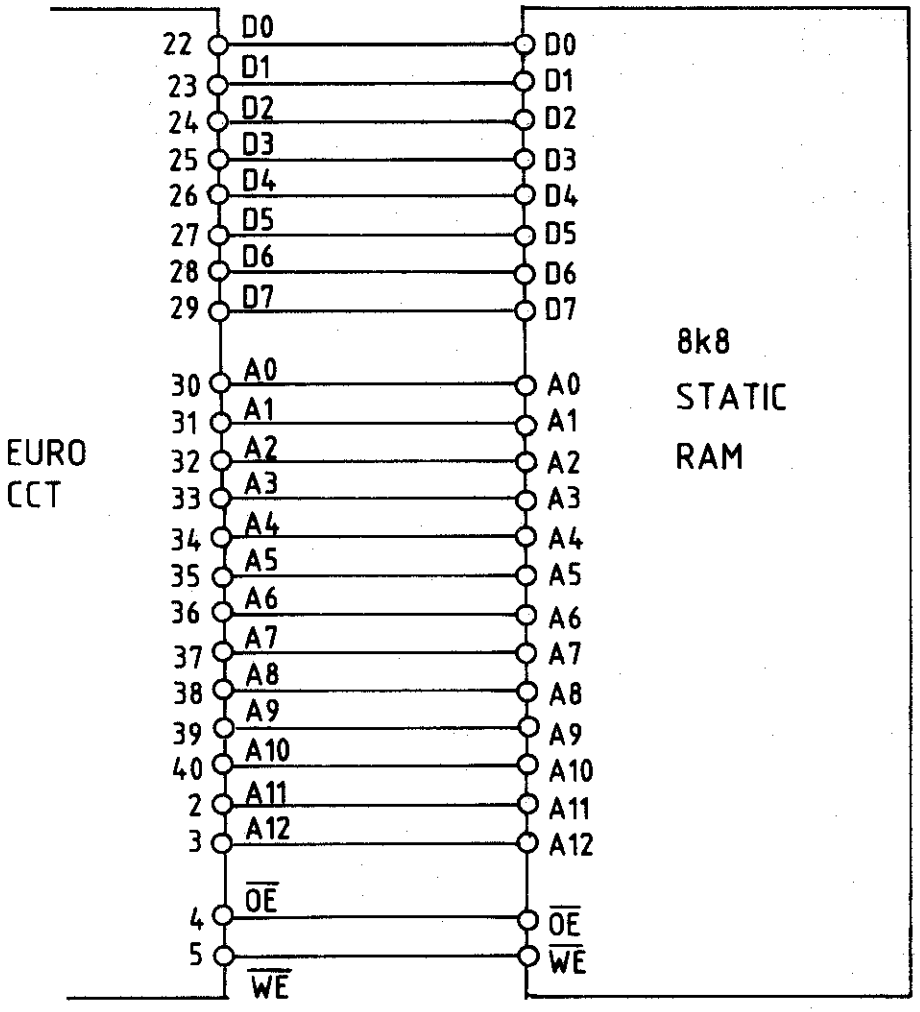


FIG. 39 INTERFACING TO 8k8 RAM

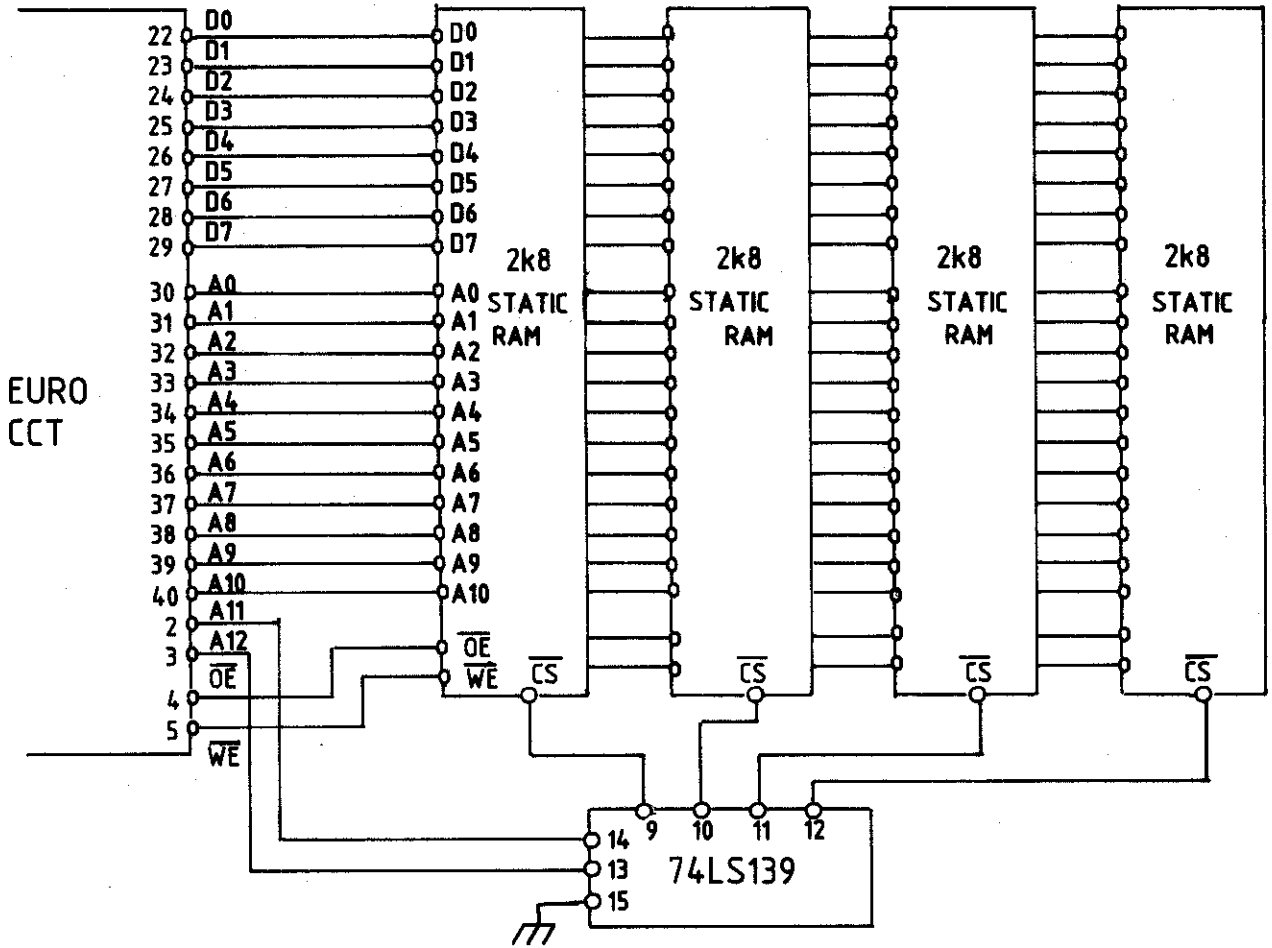
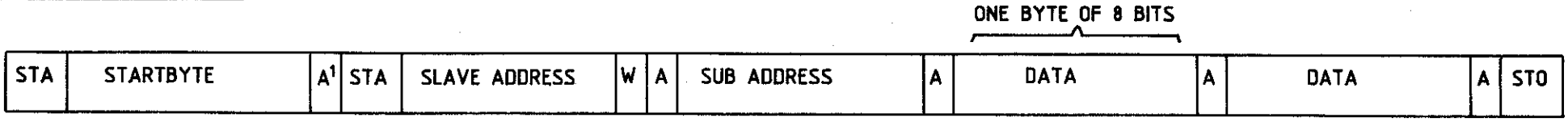


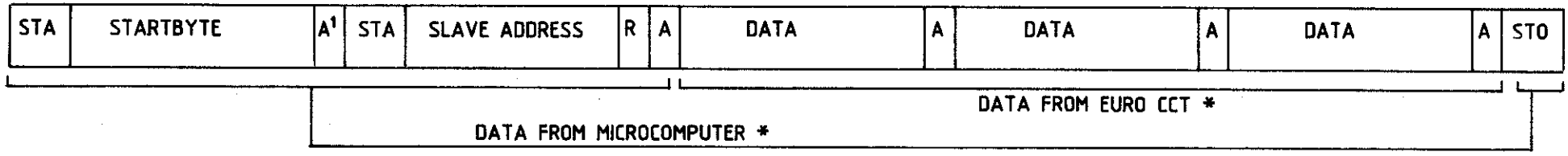
FIG. 40 INTERFACING TO FOUR 2k8 RAMS

FIG. 41 I^2C COMMAND TYPES

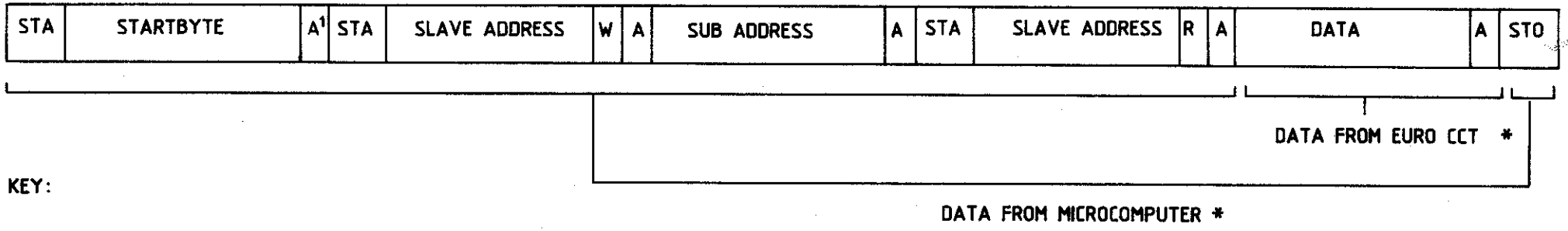
a) TRANSMITTING TO EURO CCT



b) RECEIVING FROM EURO CCT (which section of EURO CCT defined previously)



c) DEFINING SECTION THEN RECEIVING DATA FROM EURO CCT

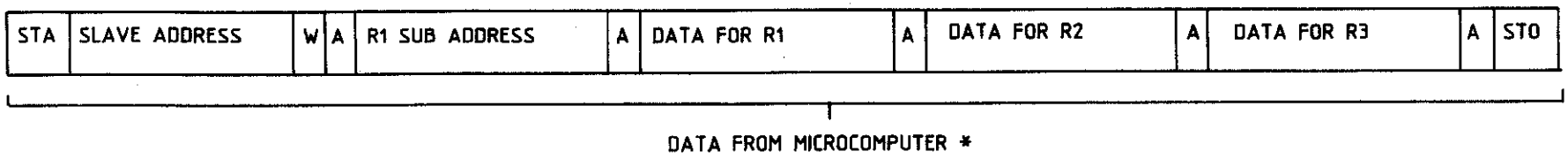


KEY:

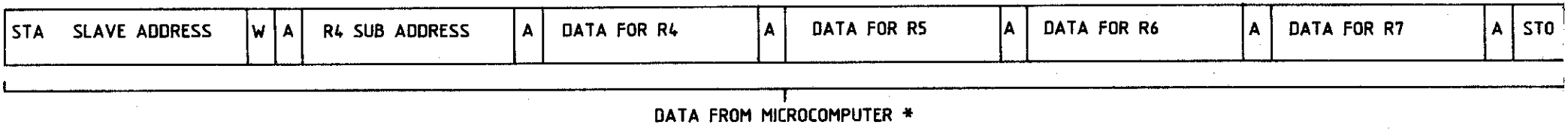
STA	Start Condition
STO	Stop Condition
A	Acknowledge
A^1	Dummy Acknowledge
*	Except Acknowledge
W	Write
R	Read

FIG. 42 EXAMPLE I^2C TRANSMISSIONS

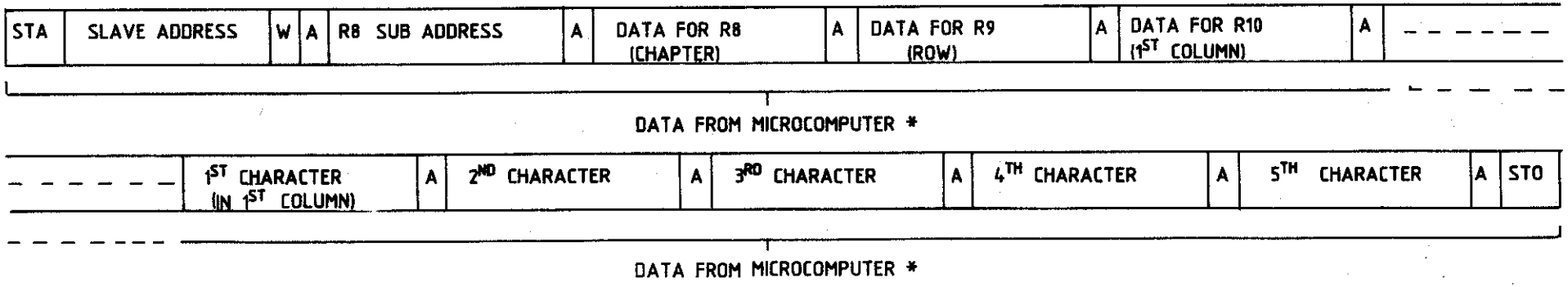
a) WRITE TO REGISTERS 1, 2 & 3



b) WRITE TO REGISTERS 4, 5, 6 & 7



c) WRITING CHARACTERS TO SCREEN USING REGISTERS 8, 9, 10 & 11



KEY:

STA	Start Condition
STO	Stop Condition
A	Acknowledge
*	Except Acknowledge Bits
W	Write

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