

# DATA SHEET

## **SAA5191** Teletext video processor

Preliminary specification  
File under Integrated Circuits, IC02

March 1991

## Teletext video processor

## SAA5191

## FEATURES

- Adaptive data slicer
- Crystal-controlled data clock regeneration with a bit rate of 6.9375 MHz
- Adaptive sync separator, horizontal phase detector and 13.5 MHz VCO to provide display phase locked loop (PLL)
- TV synchronization at teletext mode

## GENERAL DESCRIPTION

The SAA5191 is a bipolar integrated circuit that extracts teletext data from the video signal (CVBS), regenerates the teletext clock (TTC) and synchronizes the text display to the television signals (VCS). This device operates in conjunction with the Digital Video Teletext (back-end) Decoder (DVTB - SAA9042A) or any other compatible device.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage (pin 16)	–	12	–	V
$I_P$	supply current	–	70	–	mA
$V_{i\text{CVBS}}$	CVBS input signal on pin 27 (peak-to-peak value) at pin 2 LOW	–	1	–	V
	at pin 2 open-circuit	–	2.5	–	V
$V_o$	outputs signals TTC and TTD (peak-to-peak value, pins 14, 15)	2.5	3.5	4.5	V
$V_{F13}$	13.5 MHz clock output signal (peak-to-peak value pin 17)	1	2	3	V
$V_{\text{SYNC}}$	video sync output signal (peak-to-peak value, pin 1)	–	–	1	V
	SYNC output signal $\overline{\text{TCS}}$	200	450	650	mV
VCS	video composite sync level on output pin 25 LOW	–	–	0.4	V
	HIGH	2.4	–	5.5	V
$T_{\text{amb}}$	operating ambient temperature	0	–	+70	°C

## ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5191	28	DIL	plastic	SOT117 <sup>(1)</sup>

## Note

1. SOT117-1;1996 November 14

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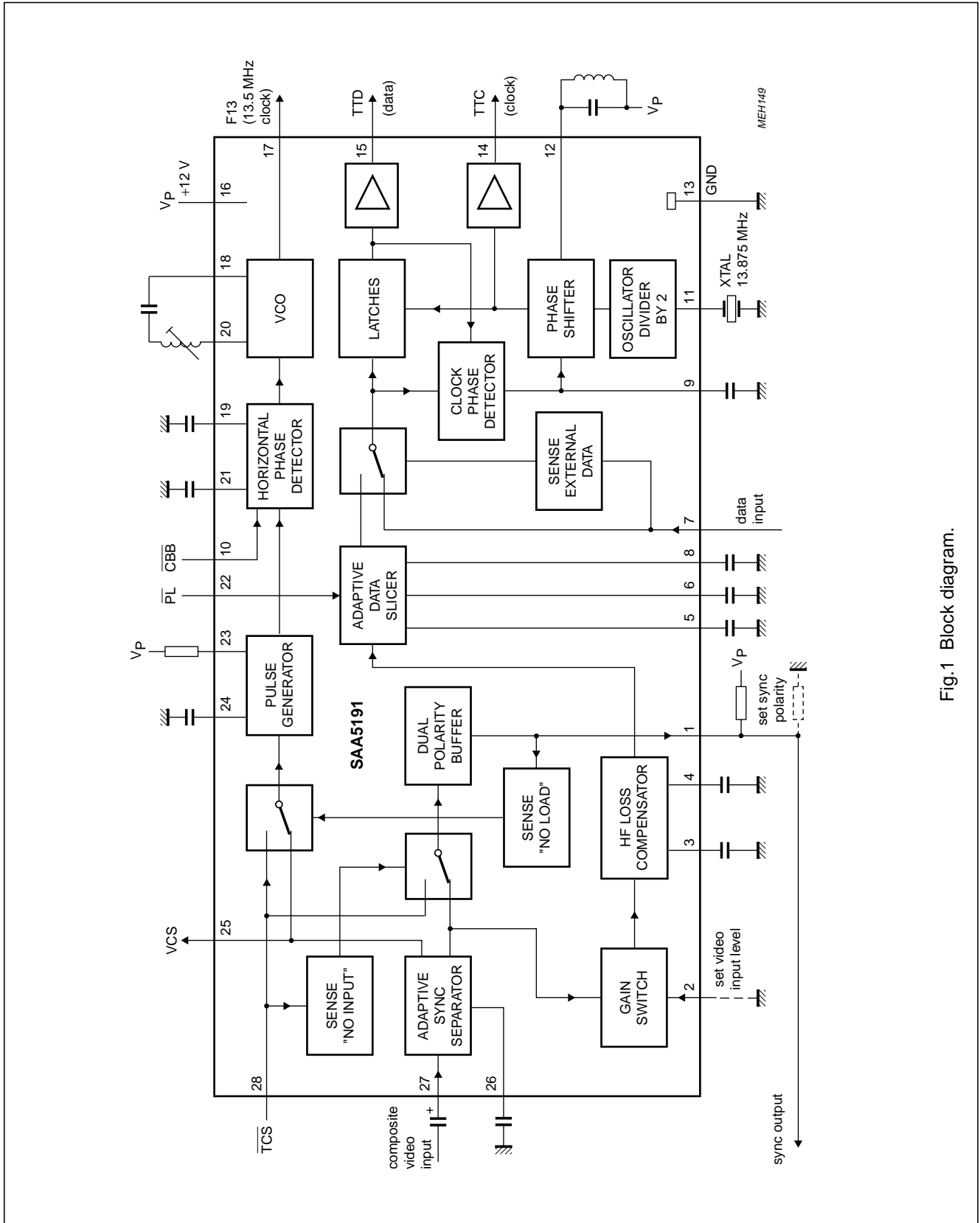


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
STTV	1	sync output signal to TV (positive or negative going)
VILS	2	level select input of video input (LOW equals 1 V)
C <sub>filt</sub>	3	video filtering capacitor of HF loss compensation
C <sub>store</sub>	4	HF storage capacitor
C <sub>ampl</sub>	5	amplitude capacitor
C <sub>zero</sub>	6	zero level capacitor
EXD	7	external data current input (note 1)
C <sub>time</sub>	8	data timing capacitor for the adaptive data slicer
C <sub>CLK</sub>	9	clock phase detector capacitor
CBB	10	blanking insertion input
XTAL	11	13.875 MHz crystal (double of data rate)
CLF	12	6.9375 MHz clock frequency filter
GND	13	ground (0 V)
TTC	14	teletext clock output (for computer controlled teletext)
TTD	15	teletext data output (for computer controlled teletext)
V <sub>P</sub>	16	+12 V supply voltage
F13	17	13.5 MHz VCO output (for sandcastle generation)
OSCO	18	oscillator output to series LC-circuit or crystal
C <sub>VCR</sub>	19	short time constant capacitor at video recorder mode (note 2)
OSCI	20	oscillator input from series LC-circuit or crystal
C <sub>hor</sub>	21	horizontal phase capacitor / VCR mode
PL	22	sandcastle input (generated in CCT)
R <sub>T</sub>	23	timing resistor for pulse generator
C <sub>T</sub>	24	timing capacitor for pulse generator
VCS	25	video composite sync output to CCT
C <sub>BL</sub>	26	black level capacitor
CVBS	27	composite video input signal from TV
TCS	28	text-composite/scan-composite sync input (TSC/SCS)

PIN CONFIGURATION

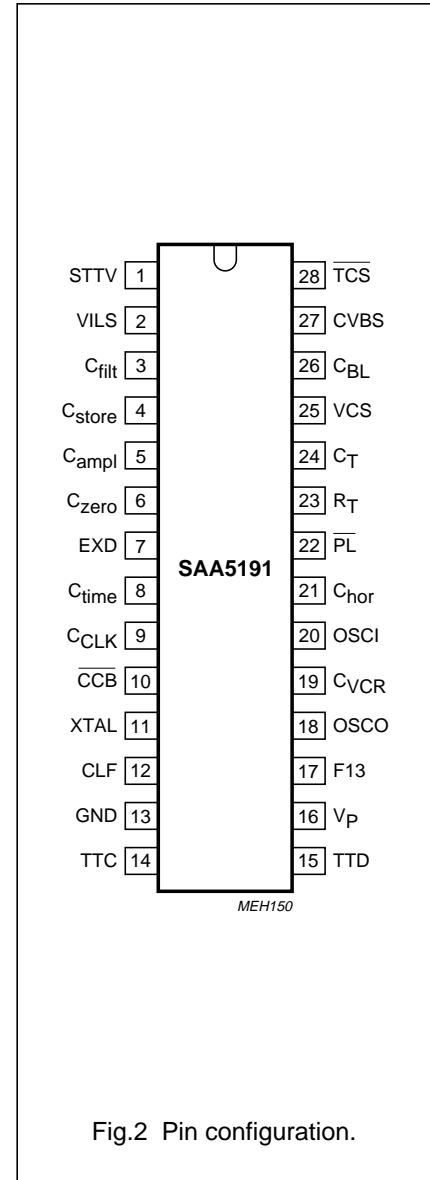


Fig.2 Pin configuration.

Notes

1. Sliced teletext data from external: active HIGH level (current), low impedance input.
2. While the loop is locking up.

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**LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_P$	supply voltage (pin 16)	0	13.2	V
$V_5$	voltage on pin 5	0	5.5	V
$T_{stg}$	storage temperature range	-20	125	°C
$T_{amb}$	operating ambient temperature range	0	+70	°C

**CHARACTERISTICS** $V_P = 12$  V;  $T_{amb} = 25$  °C and measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage range (pin 16)		10.8	12.0	13.2	V
$I_P$	supply current		50	70	105	mA
<b>Video input, sync separator and data slicer</b>		$Z_S \leq 250 \Omega$				
$V_{iCVBS}$	input signal sync to white (peak-to-peak value, pin 27)	$V_2 = \text{LOW}$	0.7	1	1.4	V
		$V_2 = \text{HIGH}$	1.75	2.5	3.5	V
	sync amplitude (peak-to-peak value) data slicing level	$V_2 = \text{LOW}$	0.1	–	1	V
		$V_2 = \text{HIGH}$	0.3	0.46	0.7	V
$V_2$	input voltage LOW (pin 2)		0	–	0.8	V
	input voltage HIGH	open-circuit equals HIGH	2.0	–	5.5	V
$I_2$	input current LOW		0	–	-150	µA
	input current HIGH	$V_2 < 5.5$ V	0	–	1	mA
<b>Teletext data output (TTD)</b>						
$V_{22}$	phase lock pulse (PL) input voltage (peak-to-peak value, pin 22)	phase locked	0	–	3	V
		phase unlocked	3.9	–	5.5	V
$V_{oTTD}$	data output signal on pin 15 (peak-to-peak value)		2.5	3.5	4.5	V
$V_{15}$	DC output voltage	mean level	3	4	5	V
$C_L$	load capacitance on pin 15		–	–	40	pF
$t_r, t_f$	rise and fall time		20	30	45	ns
<b>Teletext clock output (TTC)</b>						
$V_{oTTC}$	clock output signal on pin 14 (peak-to-peak value)		2.5	3.5	4.5	V
$V_{14}$	DC output voltage	mean level	3	4	5	V
$C_L$	load capacitance on pin 14		–	–	40	pF
$t_r, t_f$	rise and fall time		20	30	45	ns
$t_d$	delay time of falling edge relative to other edges of TTD		–	–	± 20	ns

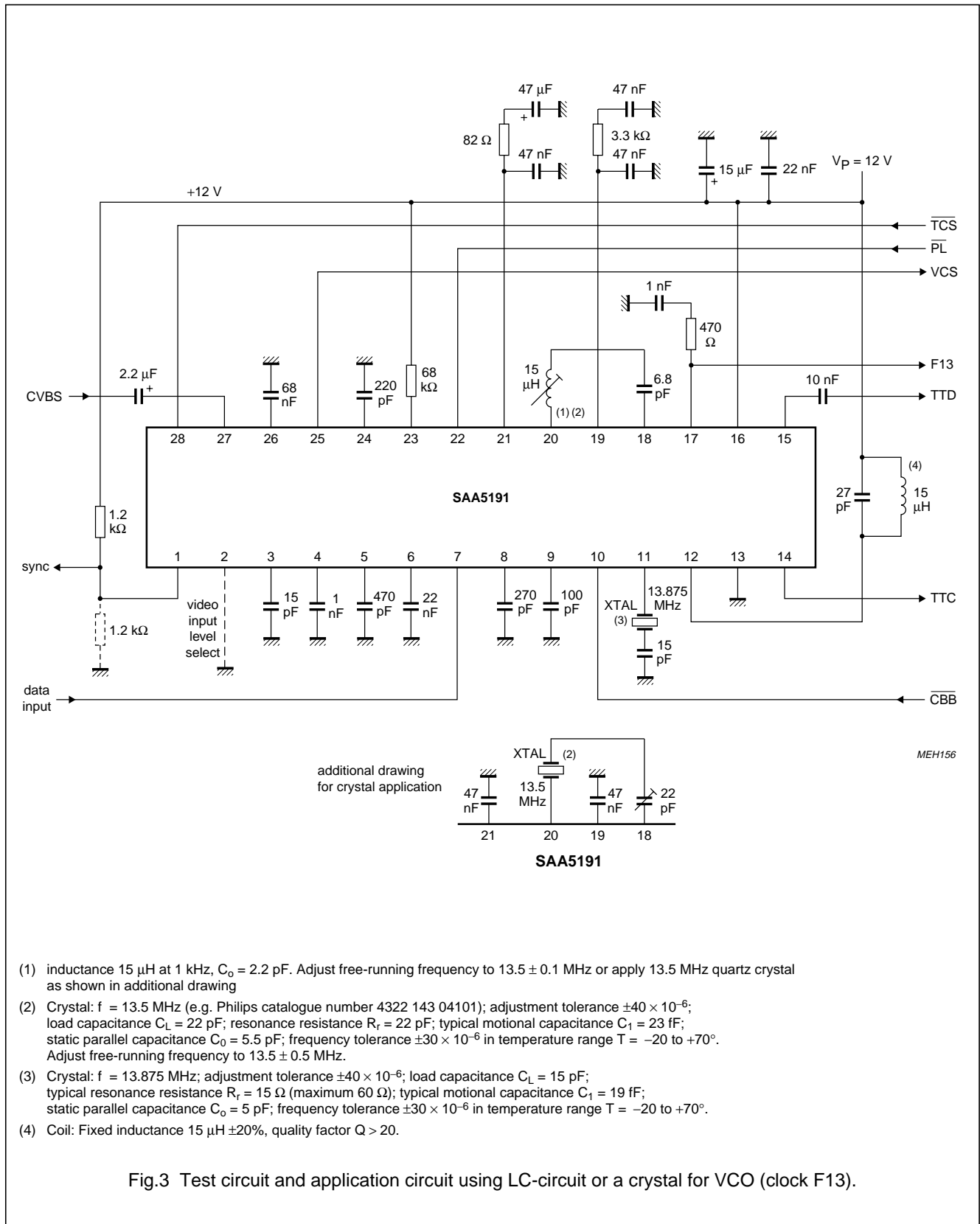
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Text/ scan composite sync input (<math>\overline{\text{TCS}}/\overline{\text{SCS}}</math>)</b>						
V <sub>28</sub>	input voltage LOW for $\overline{\text{TCS}}$ (pin 28)		0	–	0.8	V
	input voltage HIGH for $\overline{\text{TCS}}$		2.0	–	7.0	V
	input voltage LOW for $\overline{\text{SCS}}$		0	–	1.5	V
	input voltage HIGH for $\overline{\text{SCS}}$		3.5	–	7.0	V
I <sub>28</sub>	input current	V <sub>28</sub> = 0 to 7 V	–40	–70	–100	μA
		V <sub>28</sub> = 10 to V <sub>P</sub>	–	–	± 5	μA
<b>SYNC output buffer</b>						
V <sub>o</sub>	CVBS sync output signal on pin 1 (peak-to-peak value)	R <sub>L1</sub> = 1.2 kΩ to V <sub>P</sub>	–	–	1	V
	$\overline{\text{TCS}}$ output signal	R <sub>L1</sub> = 1.2 kΩ to GND	200	450	650	mV
V <sub>1</sub>	DC output voltage at positive sync signal	R <sub>L1</sub> = 1.2 kΩ to GND	1.0	1.4	2.0	V
	DC output voltage at negative sync signal	R <sub>L1</sub> = 1.2 kΩ to V <sub>P</sub>	9.0	10.1	11.0	V
I <sub>1</sub>	output current		–	–	± 3	mA
<b>Video composite sync output (VCS)</b>						
V <sub>25</sub>	output voltage LOW (pin 25)		0	–	0.4	V
	output voltage HIGH		2.4	–	5.5	V
I <sub>25</sub>	output current LOW		0	–	0.5	mA
	output current HIGH		0	–	–1.5	mA
t <sub>d</sub>	sync separator delay time		250	350	400	ns
<b>Horizontal phase detector and 13.5 MHz VCO</b>						
V <sub>10</sub>	input voltage LOW ( $\overline{\text{CBB}}$ ), pin 10	blanking inserted	0	–	0.5	V
	blanking insertion HIGH	no blanking	1.0	–	5.5	V
I <sub>10</sub>	input current		–	–	–5	μA
V <sub>o</sub>	13.5 MHz clock output signal (peak-to-peak value, pin 17)		1	2	3	V
V <sub>17</sub>	DC output voltage	maximum swing	4	–	8.5	V
C <sub>L</sub>	load capacitance on pin 17		–	–	40	pF
t <sub>r</sub> , t <sub>f</sub>	rise and fall time		10	–	30	ns

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- (1) inductance 15 μH at 1 kHz,  $C_0 = 2.2$  pF. Adjust free-running frequency to  $13.5 \pm 0.1$  MHz or apply 13.5 MHz quartz crystal as shown in additional drawing
- (2) Crystal:  $f = 13.5$  MHz (e.g. Philips catalogue number 4322 143 04101); adjustment tolerance  $\pm 40 \times 10^{-6}$ ; load capacitance  $C_L = 22$  pF; resonance resistance  $R_r = 22$  pF; typical motional capacitance  $C_1 = 23$  fF; static parallel capacitance  $C_0 = 5.5$  pF; frequency tolerance  $\pm 30 \times 10^{-6}$  in temperature range  $T = -20$  to  $+70^\circ$ . Adjust free-running frequency to  $13.5 \pm 0.5$  MHz.
- (3) Crystal:  $f = 13.875$  MHz; adjustment tolerance  $\pm 40 \times 10^{-6}$ ; load capacitance  $C_L = 15$  pF; typical resonance resistance  $R_r = 15 \Omega$  (maximum 60 Ω); typical motional capacitance  $C_1 = 19$  fF; static parallel capacitance  $C_0 = 5$  pF; frequency tolerance  $\pm 30 \times 10^{-6}$  in temperature range  $T = -20$  to  $+70^\circ$ .
- (4) Coil: Fixed inductance  $15 \mu\text{H} \pm 20\%$ , quality factor  $Q > 20$ .

Fig.3 Test circuit and application circuit using LC-circuit or a crystal for VCO (clock F13).

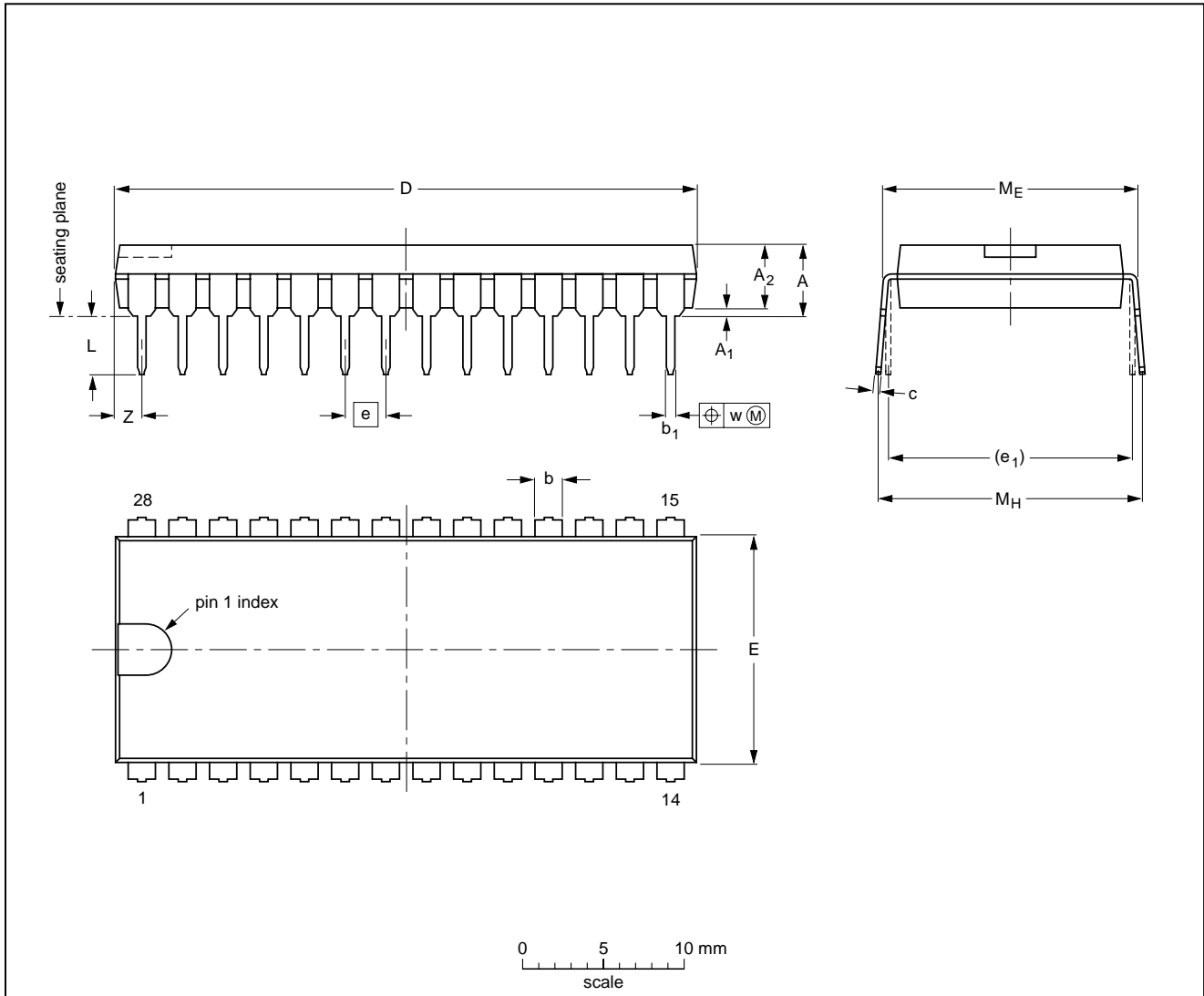
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PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				92-11-17 95-01-14



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**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

**Soldering by dipping or by wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Repairing soldered joints**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.