TELETEXT TIMING CHAIN FOR U.S.A. 525 LINE SYSTEM

The SAA5025 is an MOS N-channel integrated circuit which performs the timing functions for a teletext system.
It is a 24-lead device which provides the necessary timing signals to the teletext page memory and to the Character Generator (SAA5050 series). It works in conjunction with the Video Processor Circuit (SAA5030) and the Teletext Acquisition and Control Circuit (SAA5040 series).

Features

- Designed to operate with 525 line U.S.A. television standard (System M).
- SAA5025A for 20 row x 40 character display.
- SAA5025B for 24 row x 40 character display.
- Big Character Select input for double height characters.
- Composite sync signal output for display time-base synchronisation.
- Input clamp for a.c. coupling on "6 MHz" input.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	20	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

purpie binder, tab 6

PACKAGE OUTLINE

24-lead DIL; plastic (SOT−101A)

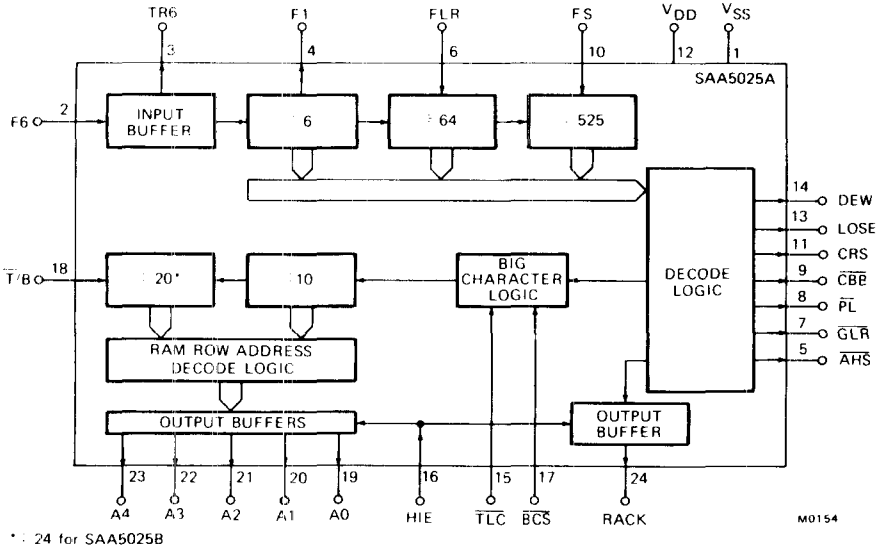


Fig.1 Block diagram.

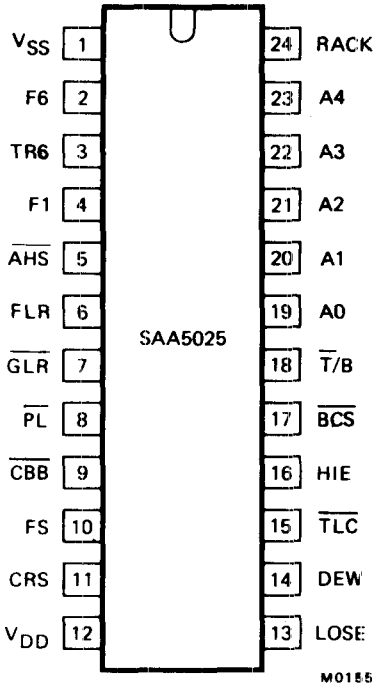


Fig.2 Pinning diagram

PINNING

no.	designation	function
1	V_{SS}	ground
2	F6	6.0419 MHz input
3	TR6	6.0419 MHz output
4	F1	1.007 MHz output
5	$\overline{AHS}$	after hours sync
6	FLR	fast line reset
7	$\overline{GLR}$	general line reset
8	$\overline{PL}$	phase lock output
9	$\overline{CBB}$	colour burst blanking
10	FS	field sync
11	CRS	character rounding select
12	V_{DD}	+5 V positive supply
13	LOSE	load output shift register enable
14	DEW	data entry window
15	$\overline{TLC}$	transmitted large character
16	HIE	high impedance enable
17	$\overline{BCS}$	big character select
18	$\overline{T}$/B	top or bottom select
19	A0	memory addresses
20	A1	
21	A2	
22	A3	
23	A4	
24	RACK	read address clock

DEVELOPMENT SAMPLE DATA

DESCRIPTION

The basic input to the SAA5025 is a 6.0419 MHz clock signal from the Video Processor Circuit (SAA5030). This clock signal is buffered and is available as an output. A divide-by-six counter produces the character rate of 1.007 MHz. This is followed by a divide-by-64 to produce the line rate and a further divide by 262/263 to derive the field rate.

The line rate is also divided by 10 to clock a counter for the teletext memory row addresses. For the SAA5025A this counter is a divide-by-20 and for the SAA5025B a divide-by-24 counter is provided. (See Fig.1).

Logic is incorporated to enable the selection of big character display, and to enable the display of transmitted large characters. An output is provided to enable character rounding for normal height characters. A composite sync signal ($\overline{AHS}$) is available as an output which can be used to synchronise the display time bases.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See 'HANDLING MOS DEVICES').

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Voltages (with respect to pin 1)

		min.	typ.	max.	
Supply voltage (pin 12)	V_{DD}	−0.3	–	7.5	V
Input voltage All inputs (pins 2,6,10,15,16,17,18)	V_I	−0.3	–	7.5	V
Output voltages (pins 3,4,5,7,11,13,14)	V_O	−0.3	–	7.5	V
(pins 16,19,20,21,23,24)	V_O	−0.3	–	7.5	V
(pins 8,9)	V_O	−0.3		13.2	V

Temperatures

Storage temperature range	T_{stg}		−20 to +125		°C
Operating ambient temperature range	T_{amb}		−20 to +70		°C

CHARACTERISTICS

Supply voltage (pin 12)	V_{DD}	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	20	50	mA
Inputs					
F6 (pin 2)					
Input voltage; HIGH	V_{IH}	2.7	–	6.5	V
Input voltage; LOW	V_{IL}	note 1	–	0	V
Rise time (between 0 V and 2.7 V levels)	t_r	–	–	30	ns
Fall time (between 0 V and 2.7 V levels)	t_f	–	–	30	ns
Mark/space ratio (measured at 1.5 V level)		44:56	50:50	56:44	
Input leakage current (V_I = 5.5 V)	I_{IR}	0.2	–	10	μA
Input leakage current (V_I = 0 V)	$-I_{IR}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
All other inputs FLR (pin 6), FS (pin 10), $\overline{TLC}$ (pin 15), HIE (pin 16), $\overline{BCS}$ (pin 17), $\overline{T/B}$ (pin 18).					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input leakage current (V_I = 0 to 5.5 V)	$\pm I_{IR}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

		min.	typ.	max.	
Outputs					
All outputs (pins 3,4,5,7,8,9,11,13, 14,19,20,21,24)					
Output node capacitance	C_O	–	–	7	pF
TR6 (pin 3)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance	C_L	–	–	15	pF
Output rise time (note 2)	t_r	–	–	30	ns
Output fall time (note 2)	t_f	–	–	30	ns
Mark/space ratio		40:60	–	60:40	
F1 (pin 4)					
Output voltage; LOW (I_{OL} = 400 μA) note 3	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time (note 2)	t_r	–	–	50	ns
Output fall time (note 2)	t_f	–	–	50	ns
Mark/space ratio		45:55	50:50	52:48	
Delay time (measured from rising edge of TR6)	t_d	7	–	60	ns
$\overline{\text{AHS}}$ (pin 5)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time (note 2)	t_r	–	–	100	ns
Output fall time (note 2)	t_f	–	–	100	ns
Delay time (falling edge measured from F1 rising edge) note 4		0	–	350	ns
$\overline{\text{GLR}}$ (pin 7)					
Output voltage; LOW (I_{OL} = 0.9 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time (note 2)	t_r	–	–	60	ns
Output fall time (note 2)	t_f	–	–	50	ns
Delay time note 4	t_d	0	–	200	ns

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

Outputs			min.	typ.	max.	
PL (pin 8) (open drain)						
Output voltage; LOW (I_{OL} = 2 mA)		V_{OL}	–	–	1.0	V
Output current in OFF state (V_O = 6 V)		I_O	–	–	10	μA
Output load capacitance		C_L	–	–	30	pF
Output fall time	note 2	t_f	–	–	100	ns
Delay time	note 4	t_d	0	–	250	ns
CBB (pin 9) (open drain)						
Output voltage; LOW (I_{OL} = 2 mA)		V_{OL}	–	–	1.0	V
Output current in OFF state (V_O = 6 V)		I_O	–	–	10	μA
Output load capacitance		C_L	–	–	30	pF
Output fall time	note 2	t_f	–	–	200	ns
Delay time	note 4	t_d	0	–	250	ns
CRS (pin 11)						
Output voltage; LOW (I_{OL} = 100 μA)		V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)		V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		C_L	–	–	30	pF
Output rise time	note 2	t_r	–	–	1	μs
Output fall time	note 2	t_r	–	–	1	μs
LOSE (pin 13)						
Output voltage; LOW (I_{OL} = 100 μA)		V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)		V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		C_L	–	–	30	pF
Output rise time	note 2	t_r	–	–	50	ns
Output fall time	note 2	t_f	–	–	50	ns
Delay time (measured from F1 falling edge)	note 4	t_d	0	–	250	ns
DEW (pin 14)						
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)		V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		C_L	–	–	50	pF
Output rise time	note 2	t_r	–	–	200	ns
Output fall time	note 2	t_f	–	–	200	ns
Delay time (measured from falling edge of $\overline{CBB}$)	note 4	t_d	6.5	6.96	7.5	μs

		min.	typ.	max.	
A0, A1, A2, A3, A4 (pins 19, 20, 21, 22 and 23) 3-state					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	85	pF
Output rise time (note 2)	t_r	–	–	1	μs
Output fall time (note 2)	t_f	–	–	1	μs
Delay time (measured from falling edge of $\overline{CBB}$) note 4	t_d	–	–	9	μs
Leakage current in OFF state (V_O = 0 to 5.5 V)	$\pm I_{IR}$	–	–	10	μA
High impedance switching times					
Into high impedance state		0	–	0.9	μs
From high impedance state		1	–	2.9	μs
RACK (pin 24) 3-state					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0		0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time (note 2)	t_r	–	–	60	ns
Output fall time (note 2)	t_f	–	–	300	ns
Delay time (measured from falling edge of F1) note 4	t_d	150	–	280	ns
Leakage current in OFF state (V_O = 0 to 5.5 V)	$\pm I_{IR}$	–	–	10	μA
High impedance switching times					
Into high impedance state		1	–	2.9	μs
From high impedance state		0	–	0.9	μs

DEVELOPMENT SAMPLE DATA

Notes

1. This input incorporates an internal clamping diode, nominal V_{IL} (min) = 0.5 V.

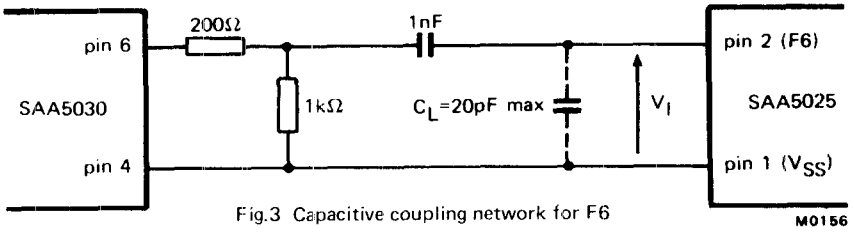


Fig.3 Capacitive coupling network for F6

2. Rise and fall times are measured between the 0.8 V and 2.0 V levels unless otherwise stated.
3. I_{OL} may be increased to 1 mA if load capacitance is less than 10 pF.
4. All delay times are measured from the rising edge of F1 unless otherwise stated.
   All delay times are measured at the 1.5 V level on the input to either the 2.0 V level on the rising edge of the output or the 0.8 V level on the falling edge of the output.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

For details of output waveforms see Fig.4.

Pin numbers

1. **V_{SS} Ground** – 0 V
2. **F6 6.0419 MHz clock input**

   Obtained from video processor (SAA5030) or other source. Permissible mark: space ratio in the range 56:44 to 40:60.
3. **TR6 6.0419 MHz clock output**

   Dot rate clock for teletext character generator (SAA5050 series).
4. **F1 1.007 MHz clock output**

   Character rate clock for teletext character generator (SAA5050 series). See Fig.4.
5. **$\overline{\text{AHS}}$ After hours sync output**

   A composite sync waveform consisting of a successive sequence of line sync pulses ($\overline{\text{LSP}}$), six equalising pulses ($\overline{\text{EP}}$), six broad pulses ($\overline{\text{BP}}$), six equalising pulses ($\overline{\text{EP}}$) and a further sequence of line sync pulses ($\overline{\text{LSP}}$). This sequence of pulses is detailed in Fig. 6.
6. **FLR Fast line reset input**

   A positive going pulse which resets the line rate counter (÷ 64). Pulse duration is between 0.5 and 63 μs. After accepting an FLR pulse further resets are inhibited for one line period, of approximately 63.5 μs.
7. **$\overline{\text{GLR}}$ General line reset output**

   A negative going pulse 993 ns wide which commences 3.97 μs after the start of each line (Fig.4).
8. **$\overline{\text{PL}}$ Phase lock output**

   This open drain output is used to lock the oscillator in the SAA5030 to the line rate. It is a negative-going pulse of duration 3.96 μs which starts at 62.02 μs on one line and ends 1.98 μs after the start of the following line (Fig.4).
9. **$\overline{\text{CBB}}$ Colour burst blanking output**

   This open-drain output blanks out the colour burst in the SAA5030. It is a 7.94 μs negative-going pulse which starts at the beginning of each line (Fig.4).
10. **FS Field sync input**

    This input accepts a positive-going pulse of approximately 160 μs duration. Its leading edge occurs during the second half of line one on even fields and correspondingly in odd fields. It is ignored during the odd field.
11. **CRS Character rounding select output**

    This signal selects character rounding in the teletext character generator (SAA5050 series). It is used for single-height characters only. The signal is HIGH during even fields (lines 1 to 263) and LOW during odd fields (lines 264 to 525).
12. **V_{DD} + 5 V positive supply**

13. **LOSE Load output shift register enable output**

This is a positive-going pulse of 39.72 μs duration commencing 13.41 μs after the start of the line period. For the SAA5025A the output is valid during lines 39 to 238 inclusive; the output is valid during lines 19 to 258 inclusive for the SAA5025B (Fig.4).

14. **DEW Data entry window output**

This signal resets the internal ROM row address counter in the SAA5050 teletext character generator. It is HIGH during lines 7 to 16 inclusive for even fields and during lines 270 to 279 inclusive for odd fields. This signal is a positive-going pulse of 636 μs duration commencing 6.95 μs after the start of the line period (Fig.5).

15. **$\overline{\text{TLC}}$ Transmitted large characters input**

When this input from SAA5050 teletext character generator is LOW it enables rows of double height characters to be displayed as required. Large characters descend into the next memory row address location.

16. **HIE High impedance enable input**

This input when taken HIGH will switch the memory row address output and read address clock (RACK) output into the high impedance state. For normal teletext operation this input should be connected to the DEW output (pin 14).

17. ***$\overline{\text{BCS}}$ Big character select input**

A signal from the SAA5040 teletext acquisition and control circuit at this input is used to enable the correct display of double-height characters, For normal size character display the input signal must be HIGH while a LOW gives double height characters.

18. ***$\overline{\text{T}}$/B Top-bottom input**

When both $\overline{\text{BCS}}$ and $\overline{\text{T}}$/B are LOW the top half of a page is displayed with double height characters. If $\overline{\text{T}}$/B is HIGH and $\overline{\text{BCS}}$ is LOW the bottom half of the page is displayed also with double height characters.

19 to 23 incl.

***A0 to A4 Memory row address outputs (3-state)**

These are binary count outputs sequencing from address 00000 (count 0) to address 10011 (count 19) for the SAA5025A (20 row) display, or to address 10111 (count 23) for the SAA5025B (24 row) display.
The binary count changes every ten lines per row in the display period of lines 39 to 238 inclusive for the 20 row display, or lines 19 to 258 inclusive for the 24 row display. The count changes between 6.5 μs and 9.0 μs after the start of the line period.

24. **RACK Read address clock input**

Provides an output to the TTL column address counter during the display period. It consists of 39 positive pulses at the 1.007 MHz rate starting at 13.57 μs after the beginning of the line period with the last negative edge occuring at 51.8 μs. This sequence is active during lines 17 to 238 inclusive for the 40 x 20 format and during lines 17 to 258 inclusive for the 40 x 24 format.

***Note**

The memory row address count depends on the states at pins 17 and 18 ($\overline{\text{BCS}}$ and $\overline{\text{T}}$/B). In the Big Character Top mode ($\overline{\text{BCS}}$ and $\overline{\text{T}}$/B are LOW) the count is 0 to 9 for the 20 row version and 0 to 11 for the 24 row version. In the Big Character Bottom mode ($\overline{\text{BCS}}$ is LOW and $\overline{\text{T}}$/B is HIGH) the row count is 10 to 19 for the 20 row version and is 12 to 23 for the 24 row version. Each Big Character row is equal to 40 tv lines.
In the Big Character Bottom mode the memory row addresses are held LOW for one line period starting 6.5 to 9.0 μs after the beginning of line 34 for the 20 row version only.

DEVELOPMENT SAMPLE DATA

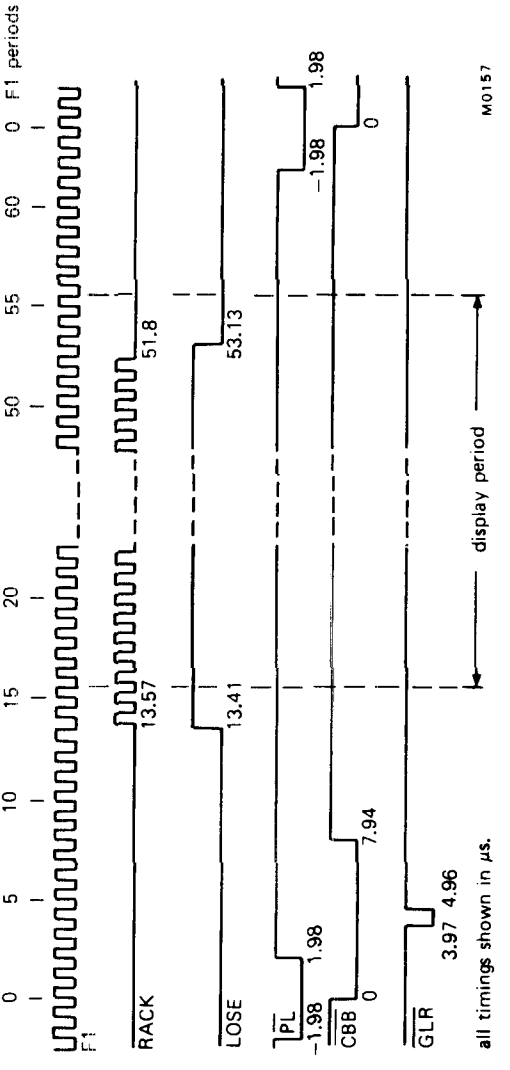


Fig.4 Line rate output waveforms.

DEVELOPMENT SAMPLE DATA

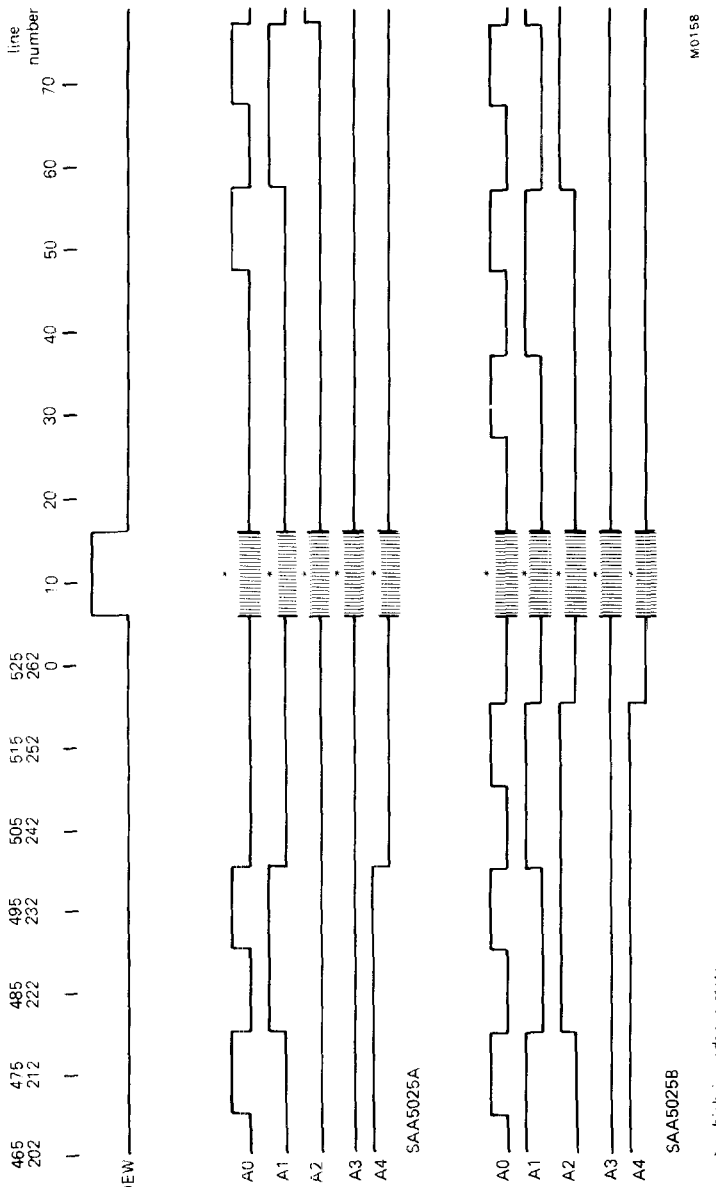
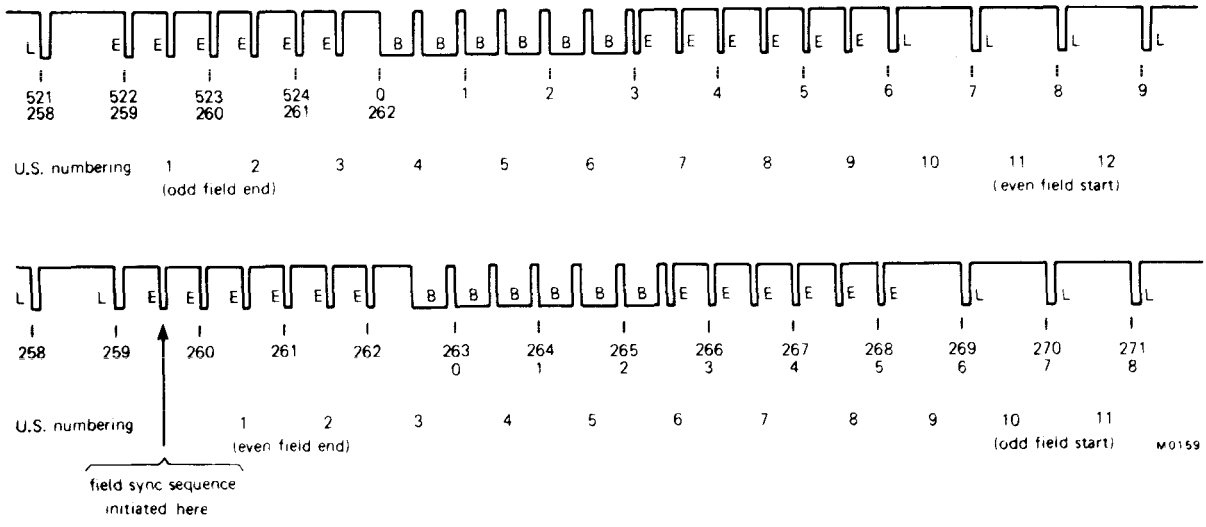


Fig.5 Timing diagram for signals decoded from field counter.



L = line sync pulses – duration 4.2 to 5.1μs

E = equalising pulses – duration 2.29 ± 10%μs

B = broad pulses – duration 26.4 to 28μs

Fig.6 After hours sync waveforms.

DEVELOPMENT SAMPLE DATA

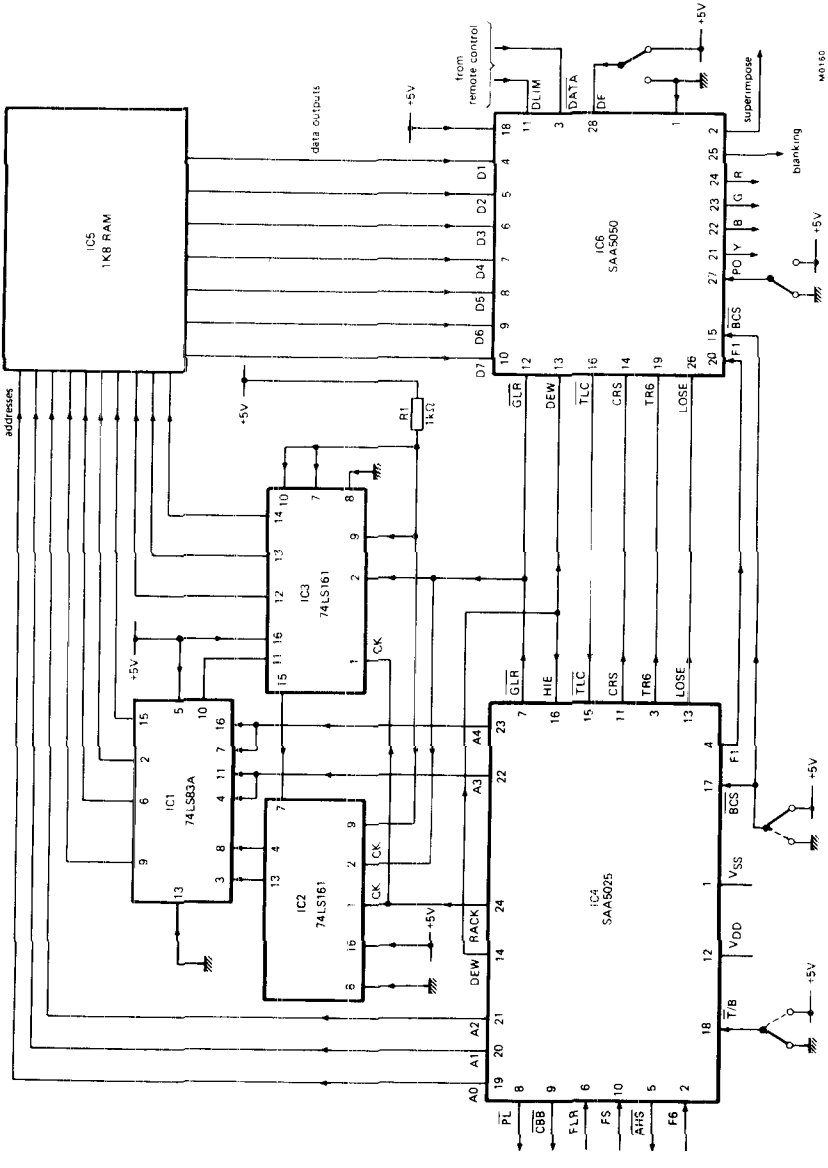
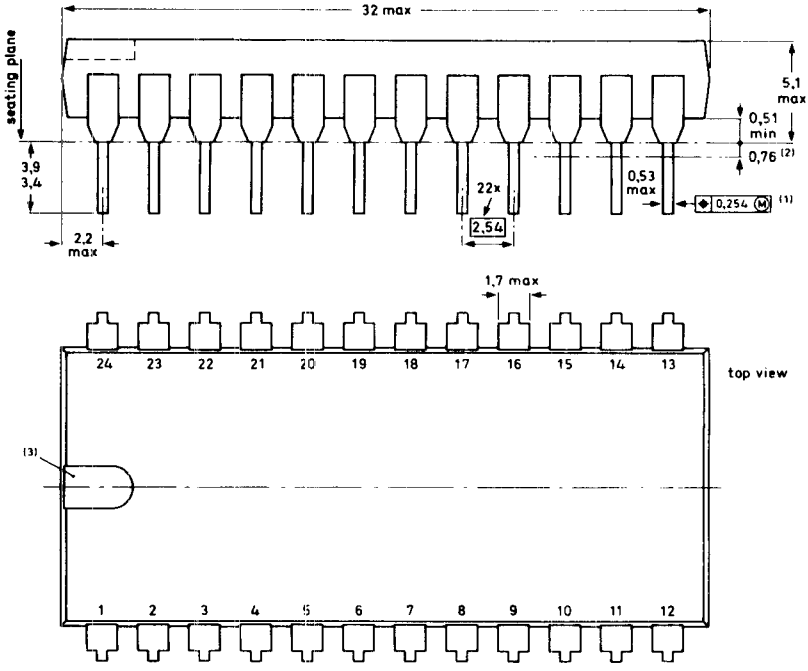
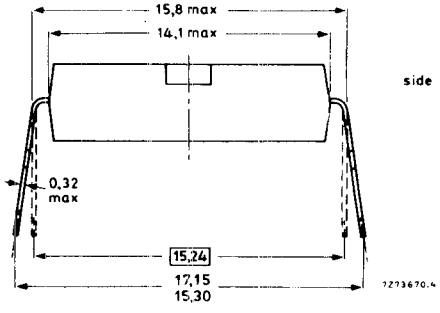


Fig.7 Timing chain and teletext character generator interface.
IC1 is a 4-bit adder used as an address converter;
IC2 and IC3 are divide-by-16 counters providing a divide-by-40 counter.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





M81-1214/11

Dimensions in mm

Positional accuracy.

Maximum Material Condition.

(1) Centre-lines of all leads are within ± 0.127 mm of the nomina. position shown; in the worst case the spacing between any two leads may deviate from nominal by ± 0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

SOLDERING

see next page

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.