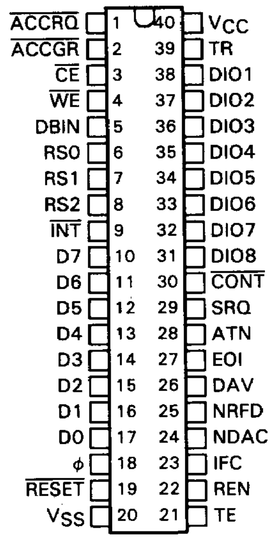
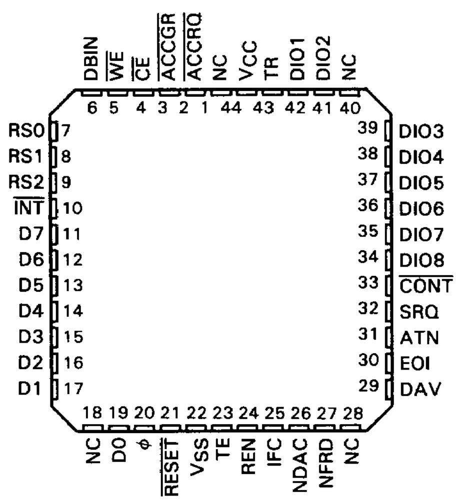
JUNE 1986 — REVISED MARCH 1988

- **Handles All IEEE-488 1975/78 Functions**
- **Compatible with IEEE-488A 1980 Supplement**
- **Maximum Transfer Rate . . . Greater Than 360 Kilobytes/Second**
- **Talker and Listener Function (T, TE, L, LE)**
- **Automatic Source and Acceptor Handshakes (SH, AH)**
- **Controller with Pass Control**
- **System Controller Capabilities**
- **Device Trigger and Device Clear Capabilities (DT, DC)**
- **Optional Automatically Cleared 'Request Service Bit'**
- **Parallel and Serial Poll Facilities (PP)**
- **Remote/Local Function with Local Lockout (RL)**
- **Single or Dual Primary Addressing**
- **Secondary Address Capabilities**
- **Direct Interface to SN75160/161/162 Bus Transceivers with No Additional Logic**
- **Compatible with Most Microprocessors**
- **Direct-Memory-Access Facilities**
- **Memory-Mapped Microprocessor Interface**
- **Temperature Range . . . −55°C to 110°C (S Suffix)**

JD PACKAGE
(TOP VIEW)



FD PACKAGE
(TOP VIEW)



description

The SMJ9914A provides an interface between a Microprocessor System and the General Purpose Interface Bus (GPIB) specified in the IEEE-488 1975/78 standards and the IEEE-488A 1980 supplement. The device is controlled and configured through 8-bit memory-mapped registers and enables all aspects of the standards to be implemented, including talker, listener and controller. The functional block diagram is shown on page 3.

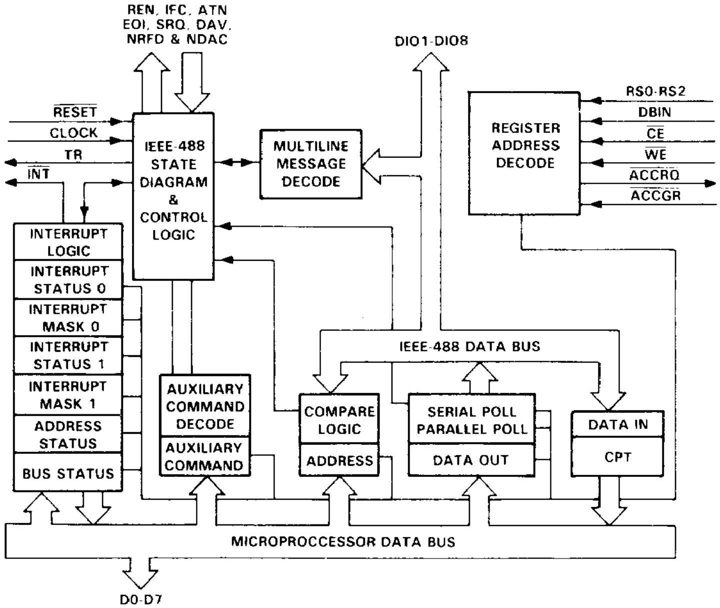
The GPIB is designed to allow up to 15 instruments within a localized area to communicate with each other over a common bus. Each device has a unique address, read from external switches at power-on, to which it responds. Information is transmitted by byte-serial bit-parallel format and may consist of either device-dependent data or interface messages, commonly referred to as data or command, respectively. A typical application is shown in Figure 1. Auxiliary commands are listed in Table 1.

Device data may be sent by any one device (the talker) and received by a number of other devices (listeners). Instructions, such as select range, select function, or measurement data for processing or printout, may be sent in this way.

The SMJ9914A performs the interface function between the microprocessor and GPIB bus and relieves the processor of the task of maintaining the IEEE protocol. By utilizing the interrupt capabilities of the device, the bus does not have to be continually polled, and fast responses to changes in the interface configuration can be achieved.

The GPIB input/output pins are connected to the IEEE-488 bus via bus tranceivers. The direction of data flow is controlled by the TE and $\overline{\text{CONT}}$ outputs generated on the SMJ9914A. The SN75160, 75161 and 75162 bus transceivers are designed specifically for use with a GPIB interface. The TE and $\overline{\text{CONT}}$ signals are routed within the devices so that the buffers on particular lines are controlled as required by the SMJ9914A. Other buffers may be used, but they may require a small amount of external logic, particularly around the EOI line buffer.

functional block diagram



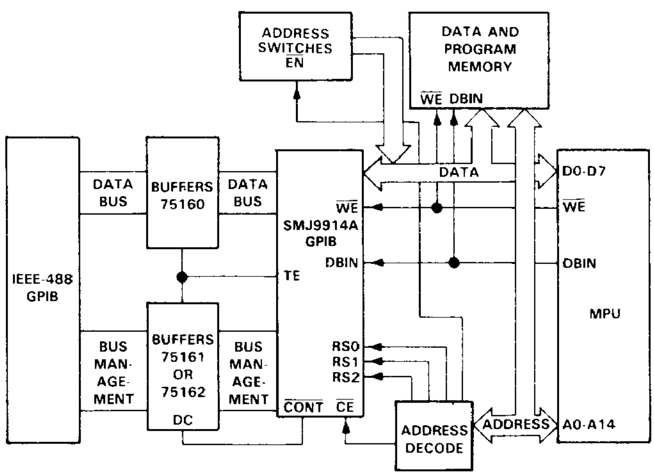


FIGURE 1. TYPICAL SMJ9914A APPLICATION

pin descriptions

PIN		I/O	DESCRIPTION
NO.	NAME	(TYPE)	
1	$\overline{ACCRQ}$	O†	Access Request. This pin becomes active (low) to request a direct memory access.
2	$\overline{ACCGR}$	I	Access Granted. When received from the direct-memory-access control logic, this enables the byte onto the data bus. $\overline{ACCGR}$ must be high when not participating in DMA transfer.
3	$\overline{CE}$	I	Chip Enable. $\overline{CE}$ allows access of read and write registers. If $\overline{CE}$ is high, D0-D7 are in high impedance unless $\overline{ACCGR}$ is low.
4	$\overline{WE}$	I	Write Enable. When active (low), indicates to the SMJ9914A that data is being written to one of its registers.
5	DBIN	I	Data Bus In. An active (high) state indicates to the SMJ9914A that a read is about to be carried out by the MPU.
6 7 8	RS0 RS1 RS2	I I I	Register Select Lines. Determine which register is addressed by the MPU during a read or write operation.
9	$\overline{INT}$	O‡	Interrupt. Sent to the MPU to cause a branch to a service routine.
17-10	D0-D7	I/O†	Data transfer lines on the MPU side of the device. D0 is the most-significant bit.
18	ϕ	I	Clock Input. 500 kHz to 5 MHz. Need not be synchronous to system clock.
19	$\overline{RESET}$§	I	Initializes the SMJ9914A at power-on.
20	V_{SS}		Ground reference voltage.
21	TE	O†	Talk Enable. Controls the direction of the transfer of the line transceivers. Logically, it is: [CACS + TACS + EIO.ATN.(CIDS + CADS) $\overline{SWRST}$].
22	REN	I/O¶	Remote Enable. Sent by system controller to select control either from the front panel or from the IEEE bus.
23	IFC	I/O¶	Interface Clear. Sent by the system controller to set the interface system into a known quiescent state. The system controller becomes the controller in charge.
24	NDAC	I/O†	Not Data Accepted. Handshake line. Acceptor sets this false (high) when it has latched the data from the I/O lines.
25	NRFD	I/O†	Not Ready For Data. Handshake line. Sent by acceptor to indicate readiness for the next byte.
26	DAV	I/O†	Data Valid. Handshake line controlled by source to show acceptors when valid data is present to the bus.
27	EOI	I/O†	End Or Identify. If $\overline{ATN}$ is false (high), this indicates the end of a message block. If $\overline{ATN}$ is true (low), the controller is requesting a parallel poll.
28	ATN	I/O†	Attention. Sent by controller in charge. When true (low), interface commands are being sent over the DIO lines. When false (high), these lines carry data.
29	SRQ	I/O†	Service Request. Set true (low) by a device to indicate a need for service.
30	$\overline{CONT}$	O†	Indicates (low) if a device is controller in charge. It is used to control direction of SRQ and ATN in pass control systems. Logically, it is (CIDS + CADS).
31-38	DIO8-DIO1	I/O†	DIO8 through DIO1 are the data input/output lines on the GPIB side. These pins connect to the IEEE-488 bus via non-inverting transceivers.
39	TR	O†	Trigger. Activated when the GET command is received over the interface or the fget command is given by the MPU.
40	V_{CC}		Supply voltage (5 V nominal).

†Push-pull output
‡Open-drain output with no internal pullup
§The hardware RESET pin has the following effect on the SMJ9914A:
- Serial and Parallel Poll registers cleared
- All clear/set auxiliary commands cleared except 'swrst'
- 'swrst' auxiliary command set. This holds the SMJ9914A in known states.

¶Open-drain output with internal pullup

Communication between the microprocessor and SMJ9914A is carried out via memory-mapped registers. There are 13 registers within the SMJ9914A, 6 of which are read and 7 are write. These registers both pass control data to and get status information from the device. These registers are listed in Table 2 and shown in Figure 2.

The three least-significant address lines from the MPU are connected to register select lines RS0, RS1, and RS2 and determine the particular register selected. The high-order address lines are decoded by external logic to cause the $\overline{CE}$ input to the SMJ9914A to be pulled low when any one of eight consecutive addresses are selected. Thus the internal registers appear to be situated at eight consecutive locations within the MPU address space. Reading or writing to these locations transfers information between the SMJ9914A and the microprocessor. Note that reading and writing to the same location will not access the same register within the SMJ9914A since they are either read-only or write-only registers. For example, a read operation with RS2-RS0 = 011 gives the current status of the GPIB interface control lines, whereas a write to this location loads the auxiliary-command register.

Each device on the bus interface is given a 5-bit address enabling it to be addressed as a talker or listener. This address is set on an external DIP switch (usually at the rear of an instrument) before power-on.

Typical SMJ9914A configuration utilizes registers 100 or 101 as an address switch register (see Table 2.). This register may consist of a DIP switch which drives the data lines via 3-state buffers when one of these addresses is read. This allows the host MPU to read a device address which is manually set and write this address into the address register of the SMJ9914A for device identification on the bus. The SMJ9914A responds by causing a My Address (MA) interrupt and entering the required addressed state when this address is detected on the GPIB data lines.

TABLE 1. AUXILIARY COMMANDS

MNEMONIC	DESCRIPTION	CLEAR	SET	C/S NA CODE
dacr	Release DAC holdoff	01	81	
dai	Disable all interrupts	13	93	
feoi	Send EOI with next byte			08
fget	Force group execute trigger	06	86	
gts	Go to standby			0B
hdfa	Holdoff on all data	03	83	
hdfe	Holdoff on EOI only	04	84	
lon	Listen only	09	89	
nbaf	New byte available false			05
pts	Pass through next secondary			14
rhdf	Release RFD holdoff			02
rlc	Release control			12
rpp	Request parallel poll	0E	8E	
rqc	Request control			11
rsv2	Request service bit 2	18	98	
rtl	Return to local	07	87	
shdw	Shadow handshake	16	96	
sic	Send interface clear	0F	8F	
sre	Send remote enable	10	90	
std1	Short T1 settling time	15	95	
tca	Take control asynchronously			0C
tcs	Take control synchronously			0D
ton	Talk only	0A	8A	
vstd1	Very short T1 delay	17	97	

TABLE 2. REGISTER ADDRESSES

ADDRESS RS2	RS1	RS0	READ REGISTERS	WRITE REGISTERS
0	0	0	Interrupt Status 0	Interrupt Mask 0
0	0	1	Interrupt Status 1	Interrupt Mask 1
0	1	0	Address Status	‡
0	1	1	Bus Status	Auxiliary Command
1	0	0	†	Address
1	0	1	†	Serial Poll
1	1	0	Command Pass Thru	Parallel Poll
1	1	1	Data In	Data Out

†The SMJ9914A host interface data lines will remain in the high-impedance state when these register locations are addressed. An Address Switch Register may therefore be included in the address space of the device at these locations.

‡This address is not decoded by the SMJ9914A. A write to this location will have no effect on the device, as if a write had not occurred.

reference documentation

- TMS9914A GPIB Controller User's Guide (SPPU013)
- TMS9914A General Purpose Interface Bus (GPIB) Controller Data Manual (MP033A)

DATA-IN REGISTER											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
1	1	1	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB

DATA-OUT REGISTER											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
1	1	1	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB

AUXILIARY-COMMAND REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	1	cs	xx	xx	f4	f3	f2	f1	f0

cs Clear or Set
f4-f0 Auxiliary command select

INTERRUPT MASK/STATUS REGISTER 0											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	xx	xx	BI	BO	END	SPAS	RLC	MAC	INT MASK 0
0	0	0	INT0	INT1	BI	BO	END	SPAS	RLC	MAC	INT STAT0

INT1 Interrupt Status Register 1
INT0 Interrupt Status Register 0
BI Byte In
BO Byte Out
END Last byte in string received
SPAS Device has been serial polled
RLC Remote/Local Change
MAC My Address Change

INTERRUPT MASK/STATUS REGISTER 1											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	INT MASK 1
0	0	1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	INT STAT 1

GET Group Execute Trigger
ERR Error
UNC Unrecognized Command
APT Address Pass Through
DCAS Device Clear Active State
SRQ Service Request
MA My Address
IFC Interface Clear

ADDRESS STATUS REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	0	REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa

REM Remote State
LLO Local Lockout
ATN Attention
LPAS Listener Primary Addressed State
TPAS Talker Primary Addressed State
LADS Addressed to listen
TADS Addressed to talk
ulpa LSB last address

ADDRESS REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
1	0	0	edpa	dal	dat	A5	A4	A3	A2	A1

edpa Enable dual-primary addressing mode
das Disable listener function
dat Disable talker function
A5-A1 Primary address

BUS STATUS REGISTER										
ADDRESS			BIT ASSIGNMENT							
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7
0	1	1	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

SERIAL POLL REGISTER											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
1	0	1	S8	rsv1	S6	S5	S4	S3	S2	S1	
			DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB

S8,S6-S1 Device Status
rsv1 Request Service bit 1

COMMAND PASS THROUGH REGISTER											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
1	1	0	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB

PARALLEL POLL REGISTER											
ADDRESS			BIT ASSIGNMENT								
RS2	RS1	RS0	D0	D1	D2	D3	D4	D5	D6	D7	
1	1	0	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	
			DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB

FIGURE 2. INTERNAL REGISTERS

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range V_{CC}‡	−0.3 V to 20 V
All input and output voltage ranges	−0.3 V to 20 V
Continuous power dissipation	1.0 W
Operating case temperature range	−55 °C to 110 °C
Storage temperature range	−55 °C to 150 °C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	All outputs except REN, IFC, $\overline{INT}$			−400	μA
		REN, IFC only			−100	μA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		−55		110	°C

electrical characteristics over full range of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs except REN,IFC,$\overline{INT}$	$I_{OH} = -400\ \mu A$	2.4			V
		REN, IFC only	$I_{OH} = -100\ \mu A$	2.2			
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.4	V
I_I	Input current (any input)		$V_{CC} = 5.25$ V, $V_I = V_{SS}$ to V_{CC}			±10	μA
I_{OZ}	Off-state output current		$V_{CC} = 5.25$ V, $V_O = 2.4$ V			20	μA
			$V_{CC} = 5.25$ V, $V_O = 0.4$ V			−20	μA
I_{CC}	V_{CC} supply current		$V_{CC} = 5.25$ V			200	mA
C_i	Input capacitance (any input)†		f = 1 MHz, all other pins at 0 V			15	pF

†Parameter guaranteed via characterization data.

clock and host interface timing requirements over full range of operating conditions

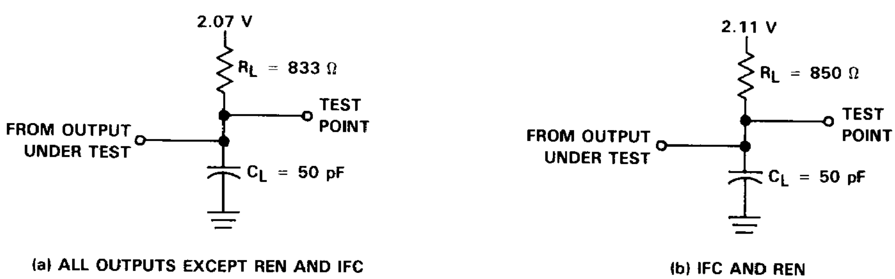
		MIN	NOM	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	200		2000	ns
$t_{w(\phi H)}$	Clock high pulse duration			1955	ns
$t_{w(\phi L)}$	Clock low pulse duration	45			ns
$t_{su(AD)}$	Address setup time	0			ns
$t_{su(DBIN)}$	DBIN setup time†	0			ns
$t_{su(CE)}$	$\overline{CE}$ setup time	100			ns
$t_{su(WE)}$	$\overline{WE}$ setup time†	0			ns
$t_{w(WE)}$	$\overline{WE}$ low pulse duration	80			ns
$t_{su(DA)}$	Data setup time	80			ns
$t_{h(DA)}$	Data hold time	15			ns
$t_{h(AD)}$	Address hold time	0			ns
$t_{h(DBIN)}$	DBIN hold time†	0			ns
$t_{h(CE)}$	$\overline{CE}$ hold time	80			ns
$t_{su(GR)}$	$\overline{ACCGR}$ setup time	100			ns
$t_{h(GR)}$	$\overline{ACCGR}$ hold time	80			ns

†Parameter guaranteed via characterization data.

host interface timing characteristics over full range of operating conditions

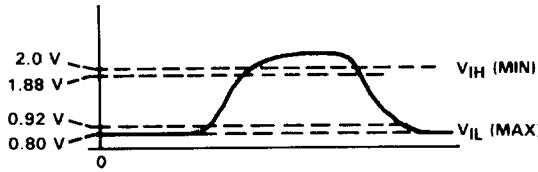
PARAMETER		MIN	NOM	MAX	UNIT
$t_{a(CE)}$	Access time from $\overline{CE}$			150	ns
$t_{a(DBIN)}$	Access time from DBIN low			150	ns
$t_{su(AD)}$	Address setup time to $\overline{CE}$	0			ns
$t_{d(DBINL\text{-}DZ)}$	DBIN low to data high impedance		50	100	ns
$t_{d(CEH\text{-}DZ)}$	$\overline{CE}$ high to data high impedance		50	100	ns
$t_{a(GR)}$	Access time from $\overline{ACCGR}$ low			150	ns
$t_{d(AGRH\text{-}DZ)}$	$\overline{ACCGR}$ high to data high impedance		50	100	ns
$t_{d(GRL\text{-}RQH)}$	Delay of $\overline{ACCRQ}$ high from $\overline{ACCGR}$ low			100	ns

PARAMETER MEASUREMENT INFORMATION

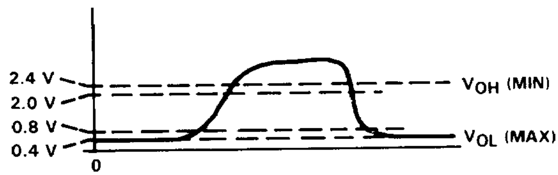


NOTE 1: Timing measurements are referenced to or from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. TEST LOAD CIRCUITS



(a) INPUT



(b) OUTPUTS

FIGURE 4. VOLTAGE REFERENCE LEVELS

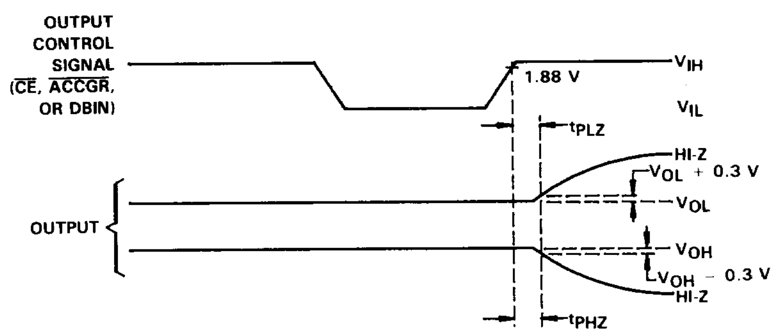
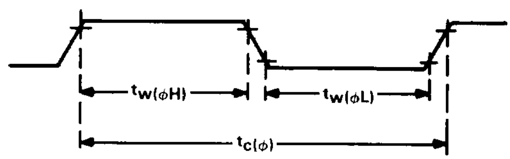
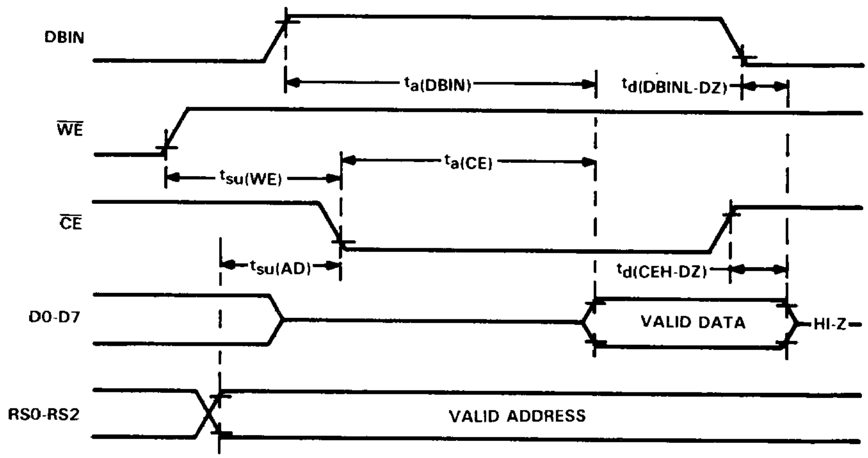


FIGURE 5. HIGH-IMPEDANCE MEASUREMENTS

clock cycle timing



read cycle timing



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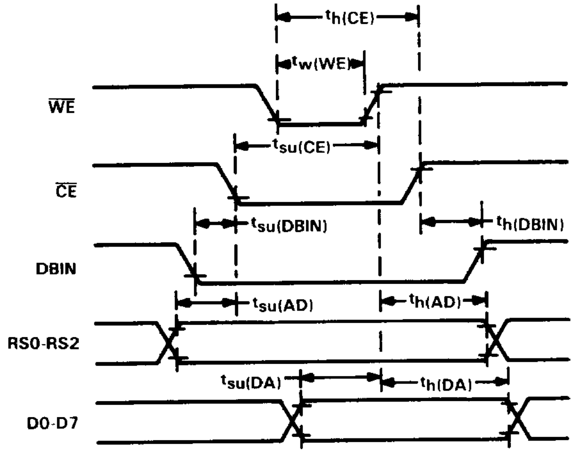
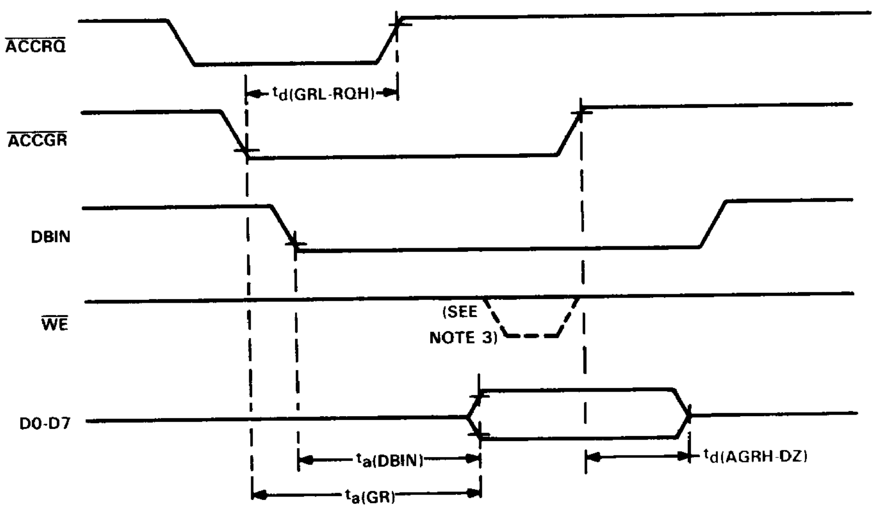
write cycle timing



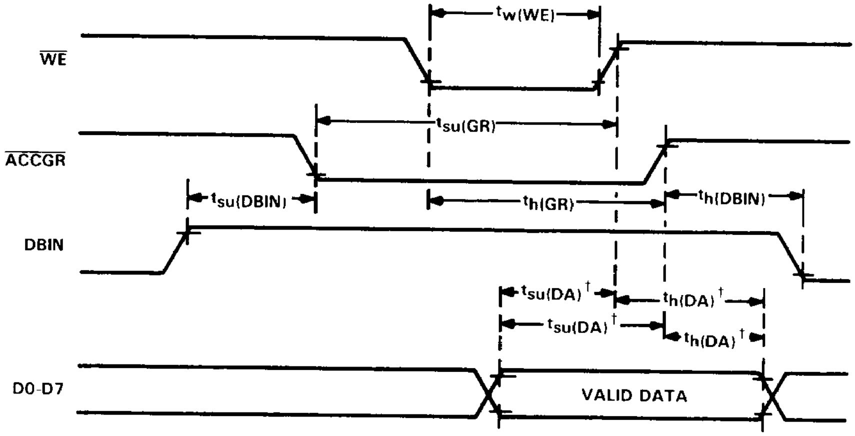
NOTE 2: $t_{h(AD)}$ and $t_{h(DA)}$ are shown measured from the rising edge of $\overline{WE}$. This is the correct reference point in this figure, since the measurements should be from the rising edge of $\overline{WE}$ or $\overline{CE}$ — whichever comes first.

DMA read operation



NOTE 3: A write-enable pulse may occur in a DMA read operation. A write-enable pulse may therefore be provided for system memory and need not be suppressed at the SMJ9914A.

DMA write operation



† $t_{su(DA)}$ and $t_{h(DA)}$ are only applicable to the first signal to become inactive, whether it is $\overline{WE}$ or $\overline{ACCGR}$.

source handshake timing characteristics over full range of operating conditions (see Note 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay of DAV true from end of write operation to data out register	Normal T_1 (see Note 5)	12(φ)↑	12(φ)↑ + 310	ns
		Short T_1 (see Note 5)	8(φ)↑	8(φ)↑ + 310	ns
		Very short T_1 (see Note 5)	4(φ)↑	4(φ)↑ + 310	ns
t_{d2}	Delay of valid GPIB data lines from end of write cycle			140	ns
t_{d3}	Delay of BO interrupt from DAC true	BO interrupt unmasked		300	ns
t_{d4}	Delay of $\overline{ACCRQ}$ DAC true			300	ns
t_{d5}	Delay of DAV false from DAC true			160	ns

NOTES: 4. The timing of the source handshake is the same whether ATN is true or false; i.e., whether the device is in TACS, CACS, or SPAS.
5. A very short bus settling time (T_1) occurs on the second and subsequent data byte when ATN is false if the "vstd1" feature is set. A slightly longer bus settling time takes place if "std1" is set unless there is a very short bus settling time. In all other instances, a normal bus settling time occurs.

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acceptor handshake timing characteristics over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d6}	Delay of BI interrupt from DAV true	BI interrupt unmasked, ATN = false, device in LACS	2(φ)↑	2(φ)↑ + 415	ns
t_{d7}	Delay of $\overline{\text{ACCRQ}}$ from DAV true	ATN = false, device is in LACS	2(φ)↑	2(φ)↑ + 290	ns
t_{d8}	Delay of NDAC false from DAV true	ATN = false, device in LACS	3(φ)↑	3(φ)↑ + 445	ns
t_{d9}	Delay of NRFD false from end of read operation of Data-In register	ATN = false, device is in LACS		220	ns
t_{d10}	Delay of interface message interupt from DAV true	ATN = false, device not in CACS, all interface message interrupts (except UNC)	2(φ)↑	2(φ)↑ + 415	ns
		UNC interrupt only	5(φ)↑	5(φ)↑ + 415	ns
t_{d11}	Delay of NDAC false from DAV true	ATN = true, device not in CACS, no DAC holdoff	7(φ)↑	7(φ)↑ + 415	ns
t_{d12}	Delay of NDAC false from end of write operation			230	ns
t_{d13}	Delay of NRFD false from DAV false	ATN = true, device not in CACS		180	ns

NOTE 6: The interrupts generated by interface messages are shown in Table 3-15 of the TMS9914A General Purpose Interface Bus (GPIB) Controller Data Manual (MP033A).

ATN, EOI, and IFC timing characteristics over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d14}	Delay of NDAC true from ATN true	Device is not in CACS		195	ns
t_{d15}	Delay of TE high from EOI true	Device is not in CACS		125	ns
t_{d16}	Delay of valid data from EOI true	Device is not in CACS		140	ns
t_{d17}	Delay of TE low from EOI false	Device is not in CACS		125	ns
t_{d18}	Delay of NRFD true from ATN false	Device is in LADS/LACS		140	ns
t_{d19}	Response time to IFC		$16t_{c(0)}$	$30t_{c(0)}$	ns

controller timing characteristics over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay of ATN true from end of tca auxiliary command		$8t_{c(0)}$	$10(\phi)$† + 220	ns
t_{d21}	Delay of BO interrupt from end of tca auxiliary command		$18t_{c(0)}$	$22(\phi)$† + 415	ns
t_{d22}	Delay of ATN true from end of tcs auxiliary command	BO unmasked, device is in ANRS	$8t_{c(0)}$	$10(\phi)$† + 220	ns
t_{d23}	Delay of BO interrupt from end of tcs auxiliary command	BO unmasked, device is in ANRS	$18t_{c(0)}$	$22(\phi)$† + 415	ns
t_{d24}	Delay of EOI true from rpp auxiliary command set			230	ns
t_{d25}	Delay of EOI false from rpp auxiliary command set			230	ns
t_{d26}	Delay of BO interrupt from rpp auxiliary command cleared	BO unmasked	$8t_{c(0)}$	$10(\phi)$† + 415	ns
t_{d27}	Delay of ATN false from gts auxiliary command	Device is not in SDYS or STRS		210	ns

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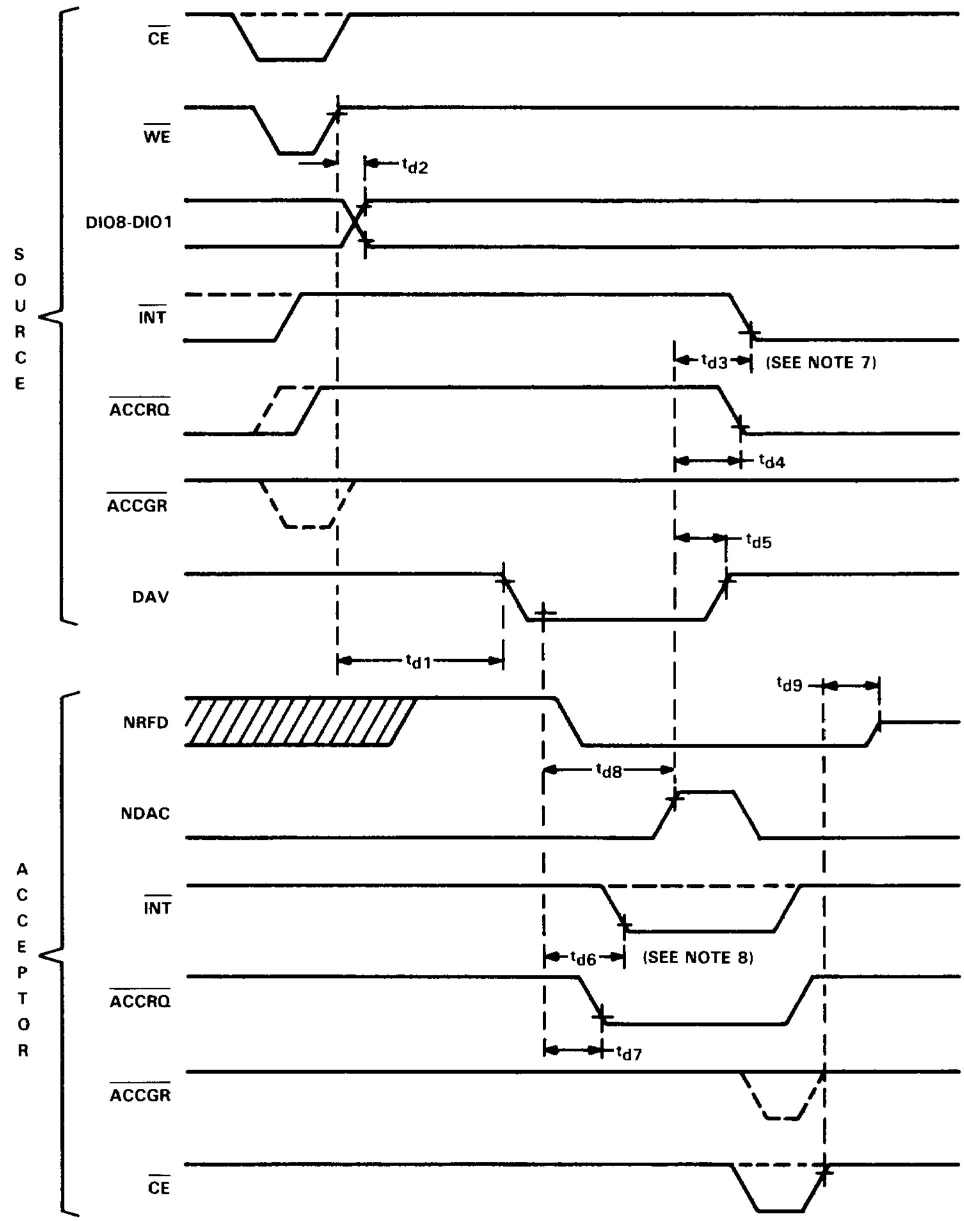
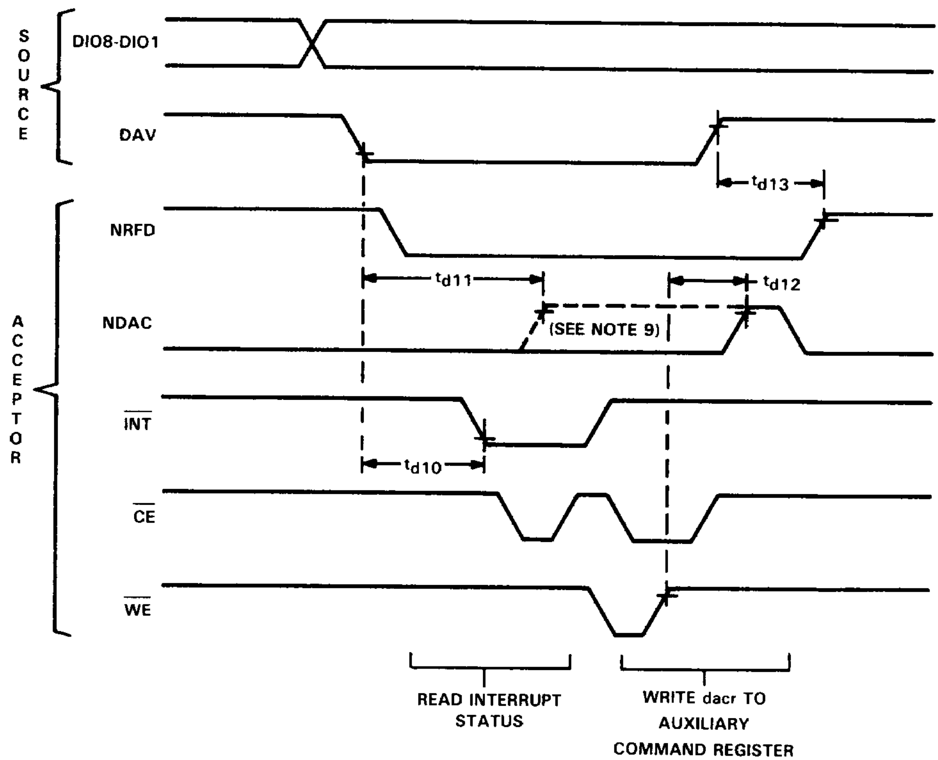
SMJ9914A source and acceptor handshake timing(s)



NOTES: 7. The interrupt line is taken low by a BO interrupt.
8. The interrupt line is taken low by a BI interrupt.

SMJ9914A acceptor handshake timing "ATN" true



NOTE 9: The broken line shows the waveform if there is no DAC holdoff. The solid lines assume there is a DAC holdoff.

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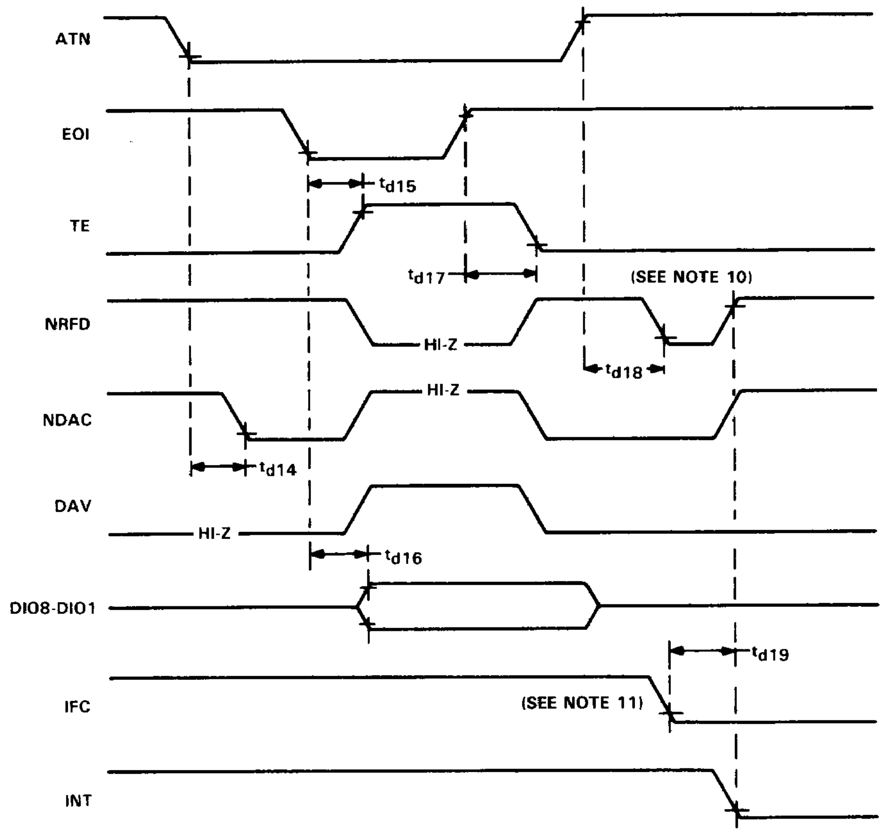
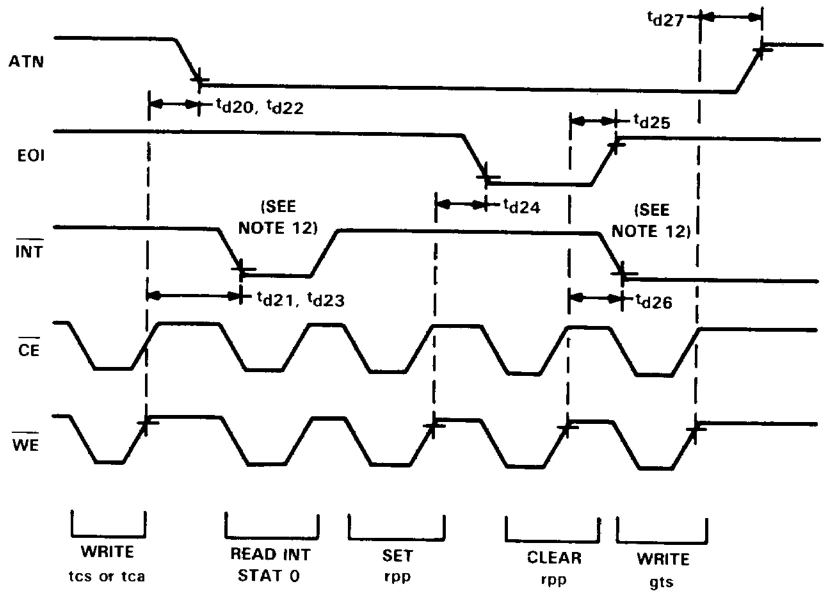
SMJ9914A response to 'ATN' and 'EOI'



NOTES: 10. This assumes that an RFD holdoff occurs.
11. IFC causes the SMJ9914A to be unaddressed and an IFC interrupt occurs.

SMJ9914A controller timing



NOTE 12: A BO interrupt occurs as the SMJ9914A enters CACS.

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