

Motorola 68000 CPU Opcodes

Mnemonic	Size	Single Effective Address	Operation	Word	Data
ORI to CCR	B	0 0 0 0	0 0 0 0	0 0 1 1 1 1	0 0 B I
ORI to SR	W	0 0 0 0	0 0 0 0	0 0 1 1 1 1	0 0 W I
ORI	B W L	0 0 0 0	0 0 0 0	S M Xn	I
ANDI to CCR	B	0 0 0 0	0 0 0 0	0 0 1 1 1 1	0 0 B I
ANDI to SR	W	0 0 0 0	0 0 0 0	0 0 1 1 1 1	0 0 W I
ANDI	B W L	0 0 0 0	0 0 0 0	S M Xn	I
SUBI	B W L	0 0 0 0	0 1 0 0	S M Xn	I
ADDI	B W L	0 0 0 0	0 1 1 0	S M Xn	I
EORI to CCR	B	0 0 0 0	1 0 1 0	0 0 1 1 1 1	0 0 B I
EORI to SR	W	0 0 0 0	1 0 1 0	0 0 1 1 1 1	0 0 W I
EORI	B W L	0 0 0 0	1 0 1 0	S M Xn	I
CMPI	B W L	0 0 0 0	1 1 0 0	S M Xn	I
BTST	B	0 0 0 0	1 0 0 0	0 0 M Xn	B N
BCHG	B	0 0 0 0	1 0 0 0	0 1 M Xn	B N
BCLR	B	0 0 0 0	1 0 0 0	1 0 M Xn	B N
BSET	B	0 0 0 0	1 0 0 0	1 1 M Xn	B N
BTST	B	0 0 0 0	Dn	1 0 0 M Xn	B N
BCHG	B	0 0 0 0	Dn	1 0 1 M Xn	B N
BCLR	B	0 0 0 0	Dn	1 1 0 M Xn	B N
BSET	B	0 0 0 0	Dn	1 1 1 M Xn	B N
MOVEP	W	0 0 0 0	Dn	1 S 0 0 1 An	W D
MOVEA	W	0 0 S	An	0 0 1 M Xn	
MOVE	B W L	0 0 S	Xn	M M Xn	
MOVE from SR	W	0 1 0 0	0 0 0 0	1 1 M Xn	
MOVE to CCR	B	0 1 0 0	0 1 0 0	1 1 M Xn	
MOVE to SR	W	0 1 0 0	0 1 1 0	1 1 M Xn	
NEGX	B W L	0 1 0 0	0 0 0 0	S M Xn	
CLR	B W L	0 1 0 0	0 0 1 0	S M Xn	
NEG	B W L	0 1 0 0	0 1 0 0	S M Xn	
NOT	B W L	0 1 0 0	0 1 1 0	S M Xn	
EXT	W	0 1 0 0	1 0 0 0	1 S 0 0 0 Dn	
NBCD	B	0 1 0 0	1 0 0 0	0 0 M Xn	
SWAP	W	0 1 0 0	1 0 0 0	0 1 0 0 Dn	
PEA	L	0 1 0 0	1 0 0 0	0 0 1 M Xn	
ILLEGAL		0 1 0 0	1 0 1 0	1 1 1 1 1 1 0 0	
TAS	B	0 1 0 0	1 0 1 0	1 1 M Xn	
TST	B W L	0 1 0 0	1 0 1 0	S M Xn	
TRAP		0 1 0 0	1 1 1 0	0 1 0 0 Vector	
LINK	W	0 1 0 0	1 1 1 0	0 1 0 0 An	W D
UNLK		0 1 0 0	1 1 1 0	0 1 0 1 An	
MOVE USP	L	0 1 0 0	1 1 1 0	0 1 1 0 An	
RESET		0 1 0 0	1 1 1 0	0 1 1 0 0 0 0	
NOP		0 1 0 0	1 1 1 0	0 1 1 0 0 0 1	
STOP		0 1 0 0	1 1 1 0	0 1 1 0 0 1 0	W I

Mnemonic	Size	Single Effective Address	Operation	Word	Data
RTE		0 1 0 0	1 1 1 0 0 1 1 1 0 0 1 1		
RTS		0 1 0 0	1 1 1 0 0 1 1 1 0 0 1 1		
TRAPV		0 1 0 0	1 1 1 0 0 1 1 1 0 1 1 0		
RTR		0 1 0 0	1 1 1 0 0 1 1 1 0 1 1 1		
JSR		0 1 0 0	1 1 1 0 1 0 1 0 M Xn		
JMP		0 1 0 0	1 1 1 0 1 0 1 1 M Xn		
MOVEM	W L	0 1 0 0	1 D 0 0 1 S M Xn	W M	
LEA	L	0 1 0 0	An 1 1 1 M Xn		
CHK	W	0 1 0 0	Dn 1 1 0 M Xn		
ADDQ	B W L	0 1 0 1	Data 0 S M Xn		
SUBQ	B W L	0 1 0 1	Data 1 S M Xn		
Scc	B	0 1 0 1	Condition 1 1 M Xn		
DBcc	W	0 1 0 1	Condition 1 1 0 0 1 Dn	W D	
BRA	B W	0 1 1 0	0 0 0 0 Displacement	W D	
BSR	B W	0 1 1 0	0 0 0 1 Displacement	W D	
Bcc	B W	0 1 1 0	Condition Displacement	W D	
MOVEQ	L	0 1 1 1	Dn 0 Data		
DIVU	W	1 0 0 0	Dn 0 1 1 M Xn		
DIVS	W	1 0 0 0	Dn 1 1 1 M Xn		
SBCD	B	1 0 0 0	Xn 1 0 0 0 0 M Xn		
OR	B W L	1 0 0 0	Dn D S M Xn		
SUB	B W L	1 0 0 1	Dn D S M Xn		
SUBX	B W L	1 0 0 1	Xn 1 S 0 0 M Xn		
SUBA	W L	1 0 0 1	An S 1 1 M Xn		
EOR	B W L	1 0 1 1	Dn 1 S M Xn		
CMPM	B W L	1 0 1 1	An 1 S 0 0 1 An		
CMP	B W L	1 0 1 1	Dn 0 S M Xn		
CMPA	W L	1 0 1 1	An S 1 1 M Xn		
MULU	W	1 1 0 0	Dn 0 1 1 M Xn		
MULS	W	1 1 0 0	Dn 1 1 1 M Xn		
ABCD	B	1 1 0 0	Xn 1 0 0 0 0 M Xn		
EXG	L	1 1 0 0	Xn 1 M 0 0 M Xn		
AND	B W L	1 1 0 0	Dn D S M Xn		
ADD	B W L	1 1 0 1	Dn D S M Xn		
ADDX	B W L	1 1 0 1	Xn 1 S 0 0 M Xn		
ADDA	W L	1 1 0 1	An S 1 1 M Xn		
ASd	B W L	1 1 1 0	0 0 0 D 1 1 M Xn		
LSd	B W L	1 1 1 0	0 0 1 D 1 1 M Xn		
ROXd	B W L	1 1 1 0	0 1 0 D 1 1 M Xn		
ROd	B W L	1 1 1 0	0 1 1 D 1 1 M Xn		
ASd	B W L	1 1 1 0	Rotation D S M 0 0 Dn		
LSd	B W L	1 1 1 0	Rotation D S M 0 1 Dn		
ROXd	B W L	1 1 1 0	Rotation D S M 1 0 Dn		
ROd	B W L	1 1 1 0	Rotation D S M 1 1 Dn		

Addressing Mode	Format	M	Xn
Data register	Dn	0 0 0	reg
Address register	An	0 0 1	reg
Address	(An)	0 1 0	reg
Address with Postincrement	(An)+	0 1 1	reg
Address with Predecrement	-(An)	1 0 0	reg
Address with Displacement	(d ₁₆ , An)	1 0 1	reg
Address with Index	(d ₈ , An, Xn)	1 1 0	reg
Program Counter with Displacement	(d ₁₆ , PC)	1 1 1 0 1 0	
Program Counter with Index	(d ₈ , PC, Xn)	1 1 1 0 1 1	
Absolute Short	(xxx)W	1 1 1 0 0 0	
Absolute Long	(xxx)L	1 1 1 0 0 1	
Immediate	#imm	1 1 1 1 0 0	

Operation Size	Suffix	S	S	S	Direction	d	D
Byte	.b	0 0	0 1	0 1	Right	R	0
Word	.w	0 1	0 1	1 1	Left	L	1
Long	.l	1 0	1 1	1 0			

Condition	Mnemonic	Cond	Rotation	M
True	T	0 0 0 0	Immediate	0
False	F	0 0 0 1	Register	1

Mode	M
Dn	0
-(An)	1

Condition	Mnemonic	Cond
Higher	HI	0 0 1 0
Lower or Same	LS	0 0 1 1
Carry Clear	CC	0 1 0 0
Carry Set	CS	0 1 0 1
Not Equal	NE	0 1 1 0
Equal	EQ	0 1 1 1
Overflow Clear	VC	1 0 0 0
Overflow Set	VS	1 0 0 1
Plus	PL	1 0 1 0
Minus	MI	1 0 1 1
Greater or Equal	GE	1 1 0 0
Less Than	LT	1 1 0 1
Greater Than	GT	1 1 1 0
Less or Equal	LE	1 1 1 1

Data Type	Letter	Data Size	Letter
Immediate	I	Byte	B
Bit Index	N	Word	W
Displacement	D	Long	L
Optional Displacement	D	Any	
Register List Mask	M		

Direction	D	D	Direction	D
Register to memory	0	1	Dn ♦ <ea> → Dn	0
Memory to register	1	0	<ea> ♦ Dn → <ea>	1

Mode	Register List Mask															
Postincrement	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Predecrement	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5	A6	A7

Brief Extension Word			
M	Xn	S	0 0 0 Displacement