Acorn A4
Technical Reference Manual

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Published by Acorn Computers Limited
ISBN 1 85250 101 4
Part number 0490,058
Issue 1, January 1993

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About this manual

This manual is intended as a hardware reference manual for the Acorn A4.

This manual supplements the basic information given on system hardware in the *Welcome Guide* and the *Portable Handbook*.

The operating system is covered at the user level in the *RISC OS 3 User Guide*, supplied with certain models (also available for separate purchase). Programmers and users requiring a greater depth of information about RISC OS will also need the *RISC OS 3 Programmer's Reference Manual*, which is available from Acorn authorised dealers.

Full details on the ARM chip set used in the computer are given in the *ARM Family Data Manual, ISBN 0-13-781618-9*, available from:

VLSI Technology, Inc.
Application Specific Logic Products Division
8375 South River Parkway
Tempe, AZ 85284
USA
602-752-8574

or from the VLSI national distributor.

Details on the 82C711 chip are available from:

Chips and Technology Inc.
3050 Zanker Road
San Jose, CA 95134
USA

Note: This manual describes various PCB assemblies. The issue of each PCB is as defined by the relevant schematic.

Part 1 – System description

Introduction

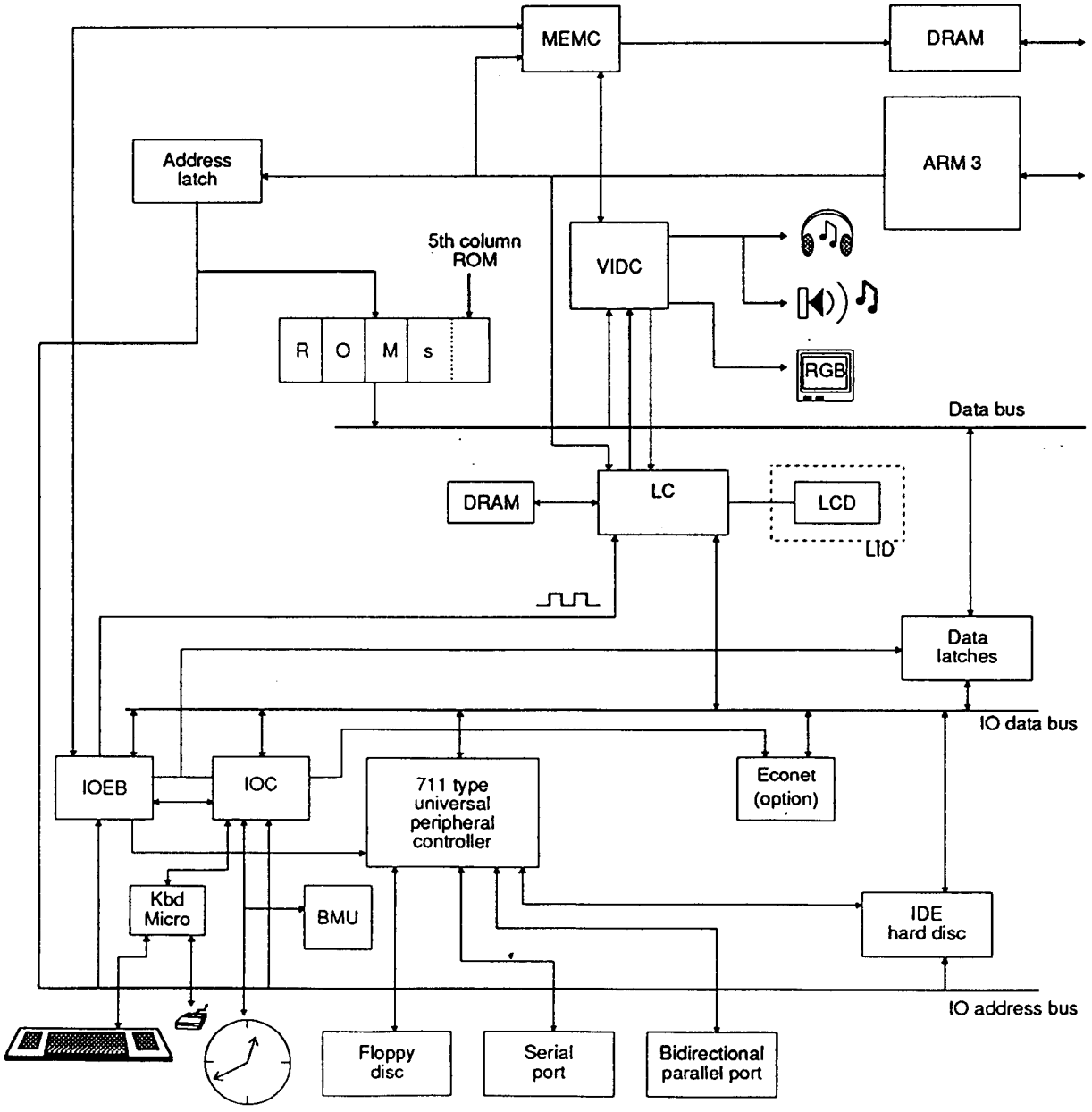
The computer is built around the ARM chip set, comprising the Advanced RISC Machine (ARM3) itself, the Memory Controller (MEMC-1A), Video Controller (VIDC) and Input/Output Controller (IOC). The memory size is configurable for 1, 2 or 4MB. A block diagram of the computer is shown below.

An ASIC (IOEB) provides much of the support and extension logic for the system. Another ASIC (LC) controls the LCD panel, and a battery management micro-controller (BMU) supports the power system.

General

The ARM3 CPU is a pipelined, 32-bit reduced instruction set microprocessor which accepts instructions and manipulates data via a high speed 32-bit data bus and 26-bit address bus, giving a 64MB uniform address space. The ARM supports virtual memory systems using a simple but powerful instruction set with good high-level language compiler support. The ARM3 has 4KB of on-chip cache memory, which greatly increases the speed with which some data is handled (typically 2 - 3 times faster than ARM2).

Figure 1.1: Block diagram of computer



MEMC acts as the interface between the ARM, VIDC, IOEB (Input/Output Extension Block), ROM (Read Only Memory) and DRAM (Dynamic RAM) devices, providing all critical system timing signals, including processor clocks.

MEMC, IOEB and IOC together control the I/O system. The internal peripherals (floppy disc, serial port, parallel port and hard disc) are all controlled by the 711 Universal Peripheral Controller chip, which itself is controlled by IOEB. IOC and IOEB control the I/O bus and expansion cards, and IOC provides basic functions such as the keyboard interface, system timers, interrupt masks and control registers. It supports a number of different peripheral cycles. All I/O accesses are memory mapped.

IOEB also contains miscellaneous registers/latches and generates the necessary signals to control ROM accesses, including the additional 5th column ROM.

Up to 4MB of DRAM can be connected to MEMC which provides all signals and refresh operations. A logical to physical translator maps the physical memory into a 32MB logical address space (with three levels of protection) allowing virtual memory and multi-tasking operations to be implemented. Fast page mode DRAM accesses are used to maximise memory bandwidth. VIDC requests data from the DRAM when required and buffers it in one of three FIFOs before using it. Data is requested in blocks of four 32-bit words, allowing efficient use of paged-mode DRAM without locking the system data bus for long periods.

MEMC supports Direct Memory Access (DMA) operations with a set of programmable DMA address generators which provide a circular buffer for video data, a linear buffer for cursor data and a double buffer for sound data. VIDC takes video data from memory under DMA control, serialises it and passes it through a colour look-up palette and converts it to analogue signals for driving the CRT guns. VIDC controls all the CRT timing parameters and controls the position and pattern of the cursor sprite. When the LCD is enabled, video data is passed from VIDC to the LCD controller (LC). LC re-times the video data, performs grey-scaling based on frame rate modulation, and generates all timing and control signals for the LCD panel. VIDC is a highly programmable device, offering a very wide choice of display formats. The colour look-up palette which drives the three on-chip DACs is 13 bits wide, offering a choice from 4096 colours or an external video source.

The cursor sprite is 32 pixels wide and any number of rasters high. Three simultaneous colours (again from a choice of 4096) are supported and any pixel can be defined as transparent, making possible cursors of many shapes. The cursor can be positioned anywhere on the screen.

The sound system implemented supports up to eight channels, each with a separate stereo position.

Also, VIDC incorporates an exponential Digital to Analogue Converter (DAC) and stereo image table for the generation of high-quality sound from data in DRAM.

System timing

Figure 1.3 on page 1-5 shows how the various clock signals are derived for the system.

MEMC divides the 36MHz clock by three to drive the memory system at 12MHz.

The ARM processor uses the 24MHz clock.

The VIDC clock is provided by LC, which selects between the 16MHz or 8MHz LCD clock, and the CRT clock provided by IOEB. IOEB provides a selection of video clock rates from 24MHz (for TV frequency modes) 25.175MHz (for VGA modes) and 36MHz (for Super VGA mode).

IOEB divides the 24MHz clock by three to produce an 8MHz clock, REF8M, which is fed to IOC, for use by 8MHz peripherals.

IOEB also divides the 24MHz clock by two to provide a 12MHz clock for the keyboard controller.

Power save mode

In power save mode, IOEB divides both the 36MHz and the 24MHz clocks by four. MEMC then uses (36/4)/3 = 3MHz, and the ARM uses 24/4 = 6MHz.

When video data is required, the MEMC clock speed flips to normal speed during the video request, then flips back to the slower power save speed.

System memory map

The system memory map is defined by MEMC, and is shown in *Figure 1.2* on page 1-4. Note that all system components, including I/O devices, are memory mapped.

I/O system

The I/O system is controlled by MEMC, IOEB and IOC. The I/O bus supports all the internal peripherals and the optional Econet expansion card.

Note: This section is intended to give the reader a general understanding of the I/O system and should not be used to program the I/O system directly. The implementation details are liable to change at any time and only the published software interfaces should be used to manipulate the I/O system. Future systems may have a different implementation of the I/O system, and in particular the addresses of locations may move. For this reason, all driver code must be relocatable.

System architecture

The I/O system consists of a 16-bit data bus (BD[0:15]), a buffered address bus (LA[2:21]), and various control and timing signals. The I/O data bus is independent of the main 32-bit system data bus, being separated from it by bidirectional latches and buffers. In this way the I/O data bus can run at much slower speeds than the main system bus to cater for slower peripheral devices. The latches between the two buses, and hence the I/O bus timing, are

controlled by the I/O controller, IOC and IOEB. IOC caters for four different cycle speeds (slow, medium, fast and synchronous). The I/O system is shown in *Figure 1.4* on page 1-6. For clarity, the data and address buses are omitted from this diagram.

Data bus mapping

The I/O data bus is 16 bits wide. Bytewide accesses are used for 8-bit peripherals. The I/O data bus (BD[0:15]) connects to the main system data bus (D[0:31]) via a set of bidirectional data latches.

The mapping of the BD[0:15] bus onto the D[0:31] bus is as follows:

- During a WRITE (i.e. ARM to peripheral) D[16:31] is mapped to BD[0:15].
- During a READ (i.e. peripheral to ARM) BD[0:15] is mapped to D[0:15].

Byte accesses

Byte instructions are used to access bytewide devices. A byte store instruction places the written byte on all four bytes of the word, and so correctly places the desired value on the lowest byte of the I/O bus. A byte or word load may be used to read a bytewide expansion card into the lowest byte of an ARM register.

Half-word accesses

To access a 16-bit wide device, half-word instructions are used. When storing, the half-word is placed on the upper 16 bits, D[16:31]. To maintain upwards compatibility with future machines, half-word stores replicate the written data on the lower half-word, D[0:15]. When reading, the upper 16 bits are undefined.

I/O space memory map

The I/O space memory map is shown in *Figure 1.5* on page 1-6.

The I/O space is controlled by IOC, MEMC and IOEB. It includes IOC controlled peripherals, the type 711 Universal Peripheral Controller. The address in I/O space determines the cycle type and the speed of the I/O access. There are basically two different types of I/O access:

- synchronised to the system memory clock (12{3}MHz) (the {3}MHz applies during power save mode)
- synchronised to the I/O clock (8MHz) whose speed is determined by IOC

IOEB determines whether an I/O access is synchronised to the 12MHz memory clock (known here as a synchronous access) by decoding address lines LA[13:18] and LA21. For synchronous accesses it enables its internal synchronous access state machine. This state machine generates an I/O cycle. The IDE drive has the capability of stretching the cycle as described below.

The following signals are generated:

- $\overline{IOR}$ Read Strobe (to 711 and IDE Hard Disc)
- $\overline{IOW}$ Write Strobe (to 711 and IDE Hard Disc)
- $\overline{FIOGT}$ Fast IO Grant handshaking signal (to MEMC)
- $\overline{BL}$ Data Bus Latch Control (read direction)
- $\overline{BLW}$ Data Bus Latch Control (write direction)
- AEN Address Enable (to 711)
- $\overline{DACK}$ Floppy Disc Data Acknowledge (to 711)
- TC Floppy Disc DMA Terminal Count signal (to 711)
- RDY IDE drive IORDY signal (internal)
- $\overline{LCDCS}$ LC controller select

All read/write accesses to the 711 and the IDE hard disc are synchronous and are all programmed I/O since MEMC1A is not capable of implementing DMA transfers to I/O space. However, a DRQ/DACK handshaking protocol (a simulated DMA cycle) is implemented with the Floppy Disc Controller section of the 711 which is used in DMA mode. This type of cycle is referred to here as a DMA cycle although this is not strictly correct. IDE hard disc accesses are programmed I/O whereas 711 accesses can be either programmed I/O or DMA cycles. Programmed I/O cycles are generated when addressing locations in the range &3010000H to &3011FFFH.

Addressing locations in the range &3012000H to &302A000H simulates DMA cycles. Each DMA cycle generates a $\overline{DACK}$ signal which the floppy driver software issues in response to a DRQ signal from the 711. The uppermost address, &302A000H, generates a TC (Terminal Count) signal in addition to a $\overline{DACK}$ signal which informs the 711 that the byte to be read/written is the last byte of the DMA transfer. The large address range in which the $\overline{DACK}$ signal is generated allows up to 24KB (i.e. sufficient for one cylinder of a 2MB floppy disc) to be transferred without resetting software pointers.

The IDE hard disc hardware interface is as used on IBM PC-AT computers. Reads and writes to the IDE registers are 8 bits wide whereas data transfers are 16 bits wide. The IDE interface is controlled by IOEB in conjunction with the 711 (which generates two chip selects, $\overline{HDCS0}$ and $\overline{HDCS1}$).

An input pin on IOEB allows the IDE hard disc to stretch the basic synchronous cycle by asserting its $\overline{IORDY}$ signal. It may do this to slow down data transfers to and from disc, for example if it does not have data ready to be read or is not ready to accept data during a write.

For all non-synchronous I/O cycles IOEB triggers its internal I/O access synchroniser. This state machine synchronises the 12MHz memory cycles to the 8MHz I/O cycles; it buffers the $\overline{FIORQ}$ and $\overline{FIOGT}$ signals from and to MEMC and generates the data bus buffer control signals ($\overline{RBE}$, $\overline{BL}$ and $\overline{BLW}$).

As stated earlier non-synchronous I/O cycles are controlled by IOC. The type and speed is determined by further address decoding and connection of address lines to IOC. IOC is connected as follows:

IOC	ARM
OE	LA21
T1	LA20
T0	LA19
B2	LA18
B1	LA17
B0	LA16

LA21 distinguishes an IOC controlled cycle (LA21=1) from a non-IOC controlled cycle (LA21 =0). Address lines connected to IOC's Type lines T[0:1] determine the cycle timing, whilst connection to IOC's Bank Select lines determines whether the access is to an IOC internal register or to a peripheral. IOC decodes B[0:3] to provide seven peripheral select lines S[1:7]. *Table 1.1* on page 1-7 shows the internal register memory map of IOC, whilst *Table 1.2* shows the peripheral address map. Note that both IOC and IOEB may all drive $\overline{BL}$. IOC controls $\overline{WBE}$ for all I/O accesses.

Figure 1.2: System memory map

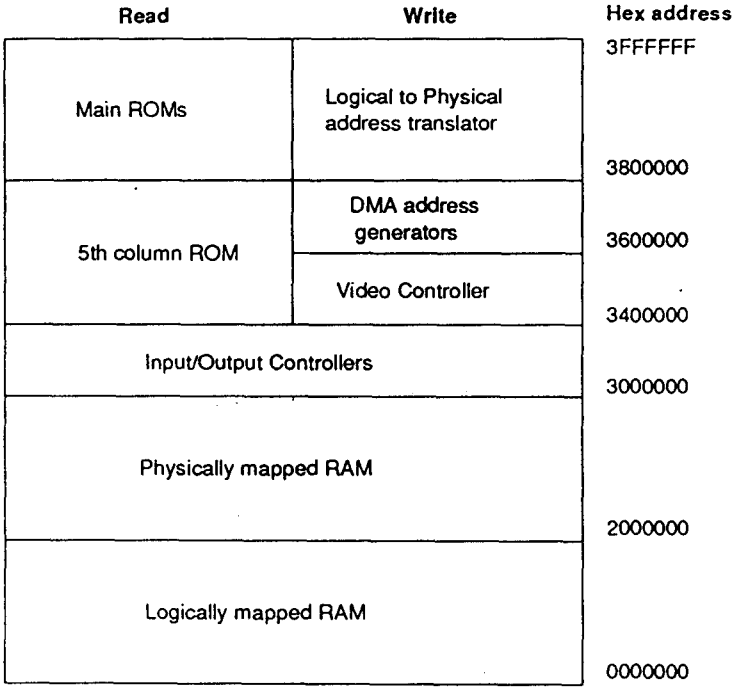


Figure 1.3: System timing

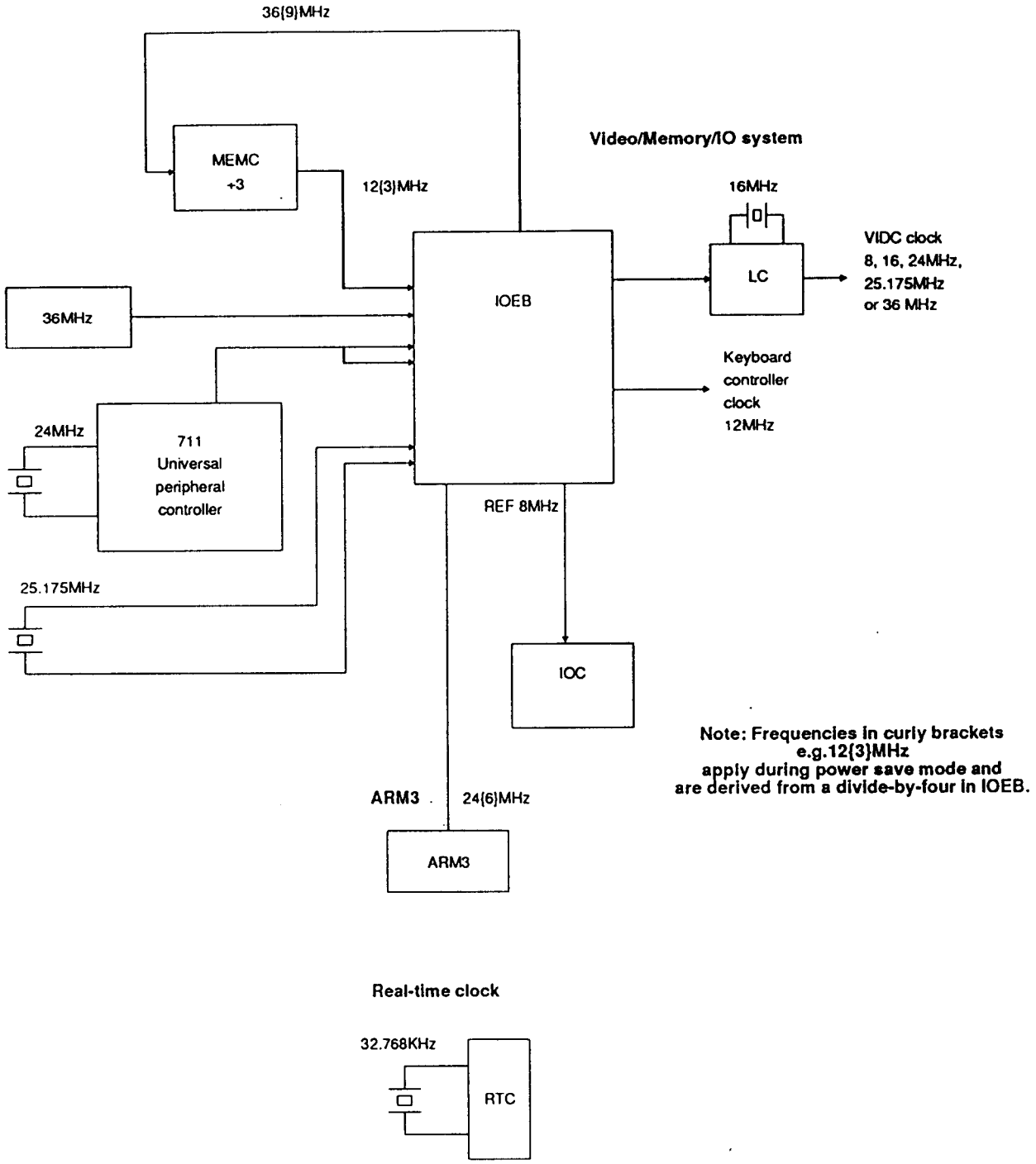


Figure 1.4: The I/O system

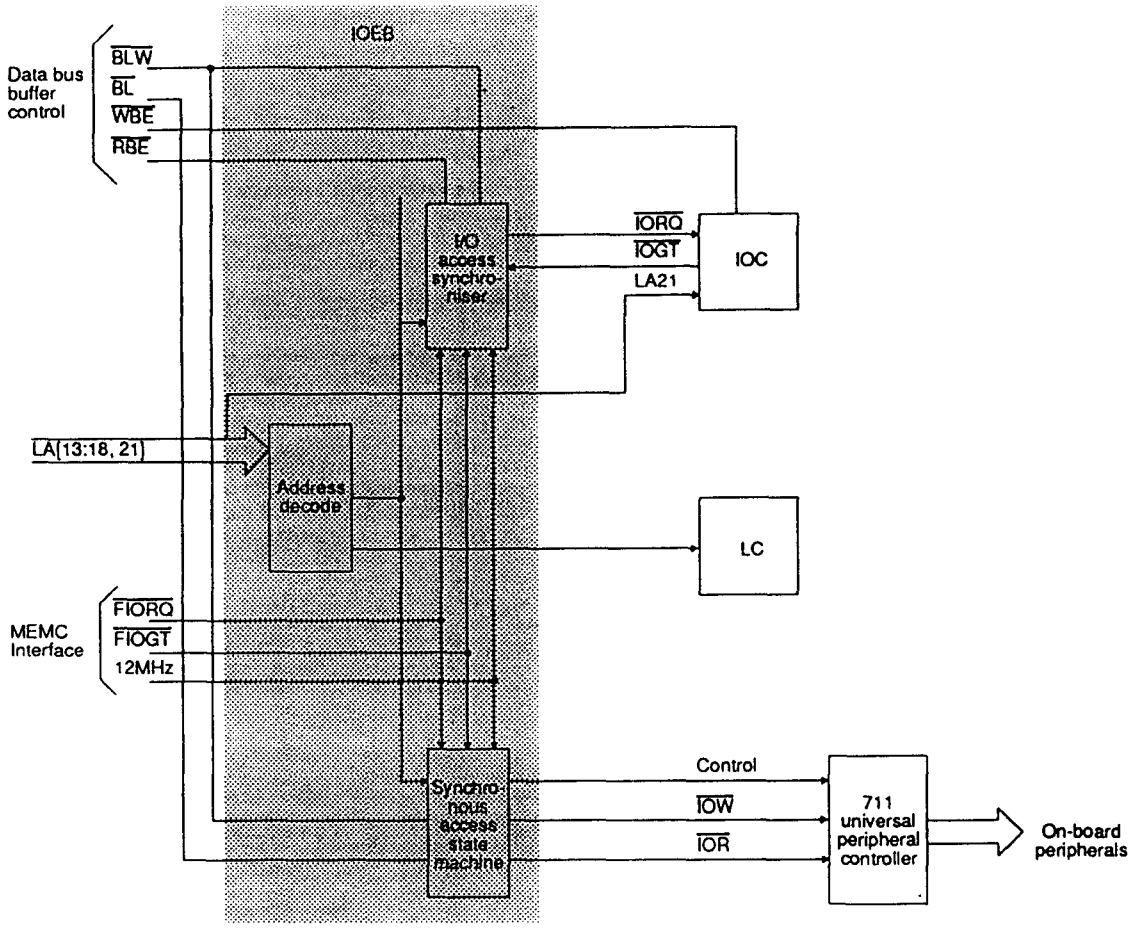


Figure 1.5: The I/O system memory map

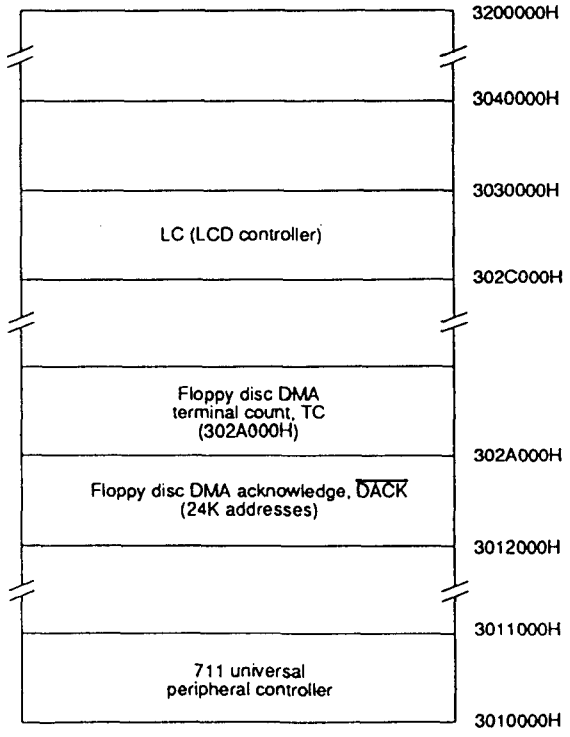


Table 1.1: Internal register memory map

Address	Read	Write
3200000H	Control	Control
3200004H	Serial Rx Data	Serial Tx Data
3200008H	-	-
320000CH	-	-
3200010H	IRQ status A	-
3200014H	IRQ request A	IRQ clear
3200018H	IRQ mask A	IRQ mask A
320001CH	-	-
3200020H	IRQ status B	-
3200024H	IRQ request B	-
3200028H	IRQ mask B	IRQ mask B
320002CH	-	-
3200030H	FIQ status	-
3200034H	FIQ request	-
3200038H	FIQ mask	FIQ mask
320003CH	-	-
3200040H	T0 count Low	T0 latch Low
3200044H	T0 count High	T0 latch High
3200048H	-	T0 go command
320004CH	-	T0 latch command
3200050H	T1 count Low	T1 latch Low
3200054H	T1 count High	T1 latch High
3200058H	-	T1 go command
320005CH	-	T1 latch command
3200060H	T2 count Low	T2 latch Low
3200064H	T2 count High	T2 latch High
3200068H	-	T2 go command
320006CH	-	T2 latch command
3200070H	T3 count Low	T3 latch Low
3200074H	T3 count High	T3 latch High
3200078H	-	T3 go command
320007CH	-	T3 latch command

Table 1.2: Peripheral address map

Cycle type	BK	Base address	IC	Use
Sync	2	&33A0000	6854	Econet controller *
Fast	5	&3350048	IOEB	Video Control Latch
Fast	5	&3350050	IOEB	IOEB Present Register
Fast	5	&3350054	IOEB	PS Latch (Reserved)
Fast	5	&3350058	IOEB	Printer Clear Register
Fast	5	&3350070	IOEB	Monitor Type Register
Fast	5	&3350074	IOEB	Latch A (reserved)
Fast	5	&3350078	IOEB	Register B
Fast	5	&335007C	IOEB	Register C

I/O programming details

This section is intended to give a general understanding of the I/O system and should not be used to program the I/O system directly. The implementation details are likely to change at any time and only published software interfaces should be used to manipulate the I/O system. Direct references to I/O addresses should never be used when programming the I/O system. The operating system determines which address is used to access a particular register or peripheral.

The following registers and latches are contained within IOEB.

Video control latch (&3350048)

This latch is a write-only register that is used by the operating system to control video sync polarity and clock speed. See *Figure 1.6.*

PS latch (&3350054)

This latch is reserved for future use.

Printer clear register(&3350058)

This is a read/write register that is used by the operating system to clear the Printer Port Interrupt Request. The Interrupt Request is cleared regardless of the value of data written.

Latch A (&3350074)

Latch A is reserved for future use.

IOEB present register (&3350050)

This is a read-only register which is used by the operating system to establish the presence of IOEB in a machine. A read will produce the bit pattern 0101 (Hex. 5) on the lower four data bits; all other bits are undefined.

Monitor type register (&3350070)

This is a read-only register which can be used to read the identity code of the monitor connected to the video connector of the computer. Standard VGA monitors use a scheme whereby four ID bits (which are either connected to GND or left open circuit in the monitor/monitor lead) are used to identify the monitor type. This scheme has been adopted and further extended to automatically sense a variety of different monitor types (see *Figure 1.7,* and *Video system* on page 1-10 for further details).

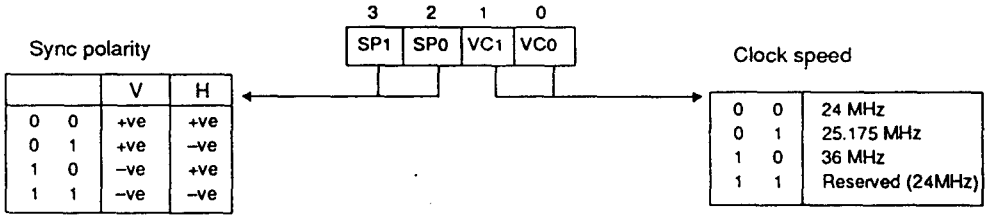
Register B (&3350078)

Register B is reserved for future use.

Register C (&335007C)

Register C is reserved for future use.

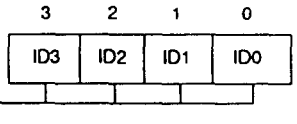
Figure 1.6: Video control latch



		V	H
0	0	+ve	+ve
0	1	+ve	–ve
1	0	–ve	+ve
1	1	–ve	–ve

0	0	24 MHz
0	1	25.175 MHz
1	0	36 MHz
1	1	Reserved (24MHz)

Figure 1.7: Monitor type register



X	1	0	1	Monochrome VGA monitor
X	1	1	0	Colour VGA monitor & some Multisync monitors
X	0	1	0	Colour VGA/Super VGA monitor & some Multisync monitors
X	HSYNC	1	1	Multisync monitors using composite sync only
X	1	1	HSYNC	TV frequency monitors/SCART TVs
X	1	1	1	No monitor connected: use LCD

X = don't care

Interrupts

The I/O system generates two independent interrupt requests, IRQ and FIQ. Interrupt requests can be caused by events internal to IOC or by external events on the interrupt or control port input pins.

The interrupts are controlled by four types of register:

- status
- mask
- request
- clear.

The status registers reflect the current state of the various interrupt sources. The mask registers determine which sources may generate an interrupt. The request registers are the logical AND of the status and mask registers and indicate which sources are generating interrupt requests to the processor. The clear register allows clearing of interrupt requests where appropriate. The mask registers are undefined after power up.

The IRQ events are split into two sets of registers, A and B. There is no priority encoding of the sources.

Internal Interrupt Events

- Timer interrupts TM[0:1]
- Power-on reset POR
- Keyboard Rx data available SRx
- Keyboard Tx data register empty STx
- Force interrupts 1.

External Interrupt Events

- IRQ active low inputs IL[0:7] wired as (0-7 respectively) PFIQ, SIRQ, SINTR, HDIRQ, FINTR, PIRQ, LPINTR, with IL7 not used
- IRQ falling-edge input IF wired as INDEX
- IRQ rising-edge input IR wired as VFLYBK
- FIQ active high inputs FH[0:1] wired as FDDRQ with FH1 not used
- FIQ active low input FL wired as EFIQ
- Control port inputs C[3:5].

Table 1.3: IRQ status A

Bit	Name	Function
0	LPINTR	Parallel port latched interrupt
1	-	Not used
2	INDEX	Start of floppy disc index pulse
3	VFLYBK	Start of display vertical flyback
4	POR	Power-on reset has occurred
5	TM0	Timer 0 event, latched
6	TM1	Timer 1 event, latched
7	FORCE	Software generated IRQ

Table 1.4: IRQ status B

Bit	Name	Function
0	PFIQ	Podule FIQ request
1	SIRQ	Sound buffer pointer used
2	SINTR	Serial line interrupt
3	HDIRQ	Hard disc interrupt
4	FINTR	Floppy disc interrupt
5	PIRQ	Podule IRQ request
6	STX	Keyboard transmit register empty
7	SRX	Keyboard receive register full

Table 1.5: FIQ Interrupt status

Bit	Name	Function
0	FDDRQ	Floppy Disc Data Request
1	-	not used
2	EFIQ	Econet Interrupt Request
3	C3	Used as an I/O bit
4	SINTR	Serial Line interrupt
5	-	not used
6	PFIQ	Podule FIQ request
7	Force	Software generated FIQ interrupt

Control port

The control register allows the external control pins C[0:5] to be read and written and the status of the $\overline{\text{INDEX}}$ and VFLY inputs to be inspected. The C[0:5] bits manipulate the C[0:5] I/O port. When read, they reflect the current state of these pins. When written LOW the output pin is driven LOW. These outputs are open-drain, and if programmed HIGH the pin is undriven and may be treated as an input.

Table 1.6: Control register bit settings

Bit	Name	Function
C7	VFLYBK	Allows the state of VFLYBK to be inspected. Reads HIGH during vertical flyback and LOW during display. See VIDC data sheet for details. This bit MUST be programmed HIGH for normal system operation.
C6	INDEX	Allows the state of the floppy disc drive $\overline{\text{INDEX}}$ signal to be inspected. This bit MUST be programmed HIGH for normal operation.
C5	SMUTE	This controls the muting of the internal speaker. It is programmed HIGH to mute the speaker and LOW to enable it. The speaker is muted on reset.
C4	SINTR	Used as the Serial Line Interrupt Request, and must be programmed HIGH.
C3	C3	Reserved for future use.
C2	C2	Reserved for future use.
C[1:0]	SDA, SCL	Used to implement the bi-directional serial I2C bus to the Real Time Clock.

Sound system

The sound system is based on the VIDC stereo sound hardware. External analogue anti-alias filters are used which are optimised for a 20 kHz sample rate. The sound output is available from a 3.5mm stereo jack socket which will directly drive personal stereo headphones, or, alternatively, an amplifier and speakers. One internal speaker is fitted, to provide mono audio.

VIDC sound system hardware

VIDC contains an independent sound channel consisting of the following components: A four-word FIFO buffers 16 8-bit sound samples, with a DMA request issued whenever the last byte is consumed from the FIFO. The sample bytes are read out at a constant sample rate programmed into the 8-bit Audio Frequency Register. This may be programmed to allow samples to be output synchronously at any integer value between 3 and 255 microsecond intervals.

The sample data bytes are treated as sign plus 7-bit logarithmic magnitude and, after exponential digital to analogue conversion, de-glitching and sign-bit steering, are output as a current at one of the audio output pins to be integrated and filtered externally.

VIDC also contains a bank of eight stereo image position registers, each of three bits. These eight registers are sequenced through at the sample rate with the first register synchronised to the first byte clocked out of the FIFO. Every sample time is divided into eight time slots and the 3-bit image value programmed for each register is used to pulse width modulate the output amplitude between the LEFT and RIGHT audio current outputs in multiples of time slot subdivisions. This allows the signal to be spatially positioned in one of seven stereo image positions.

MEMC sound system hardware

MEMC provides three internal DMA address registers to support sound buffer output; these control the DMA operations performed following Sound DMA requests from VIDC. The registers allow the physical addresses for the START, PNTR (incremental) and END buffer pointers to a block of data in the lowest half megabyte of physical RAM to be accessed.

These operate as follows: programming a 19-bit address into the PNTR register sets the physical address from which sequential DMA reads will occur (in multiples of four words), and programming the END pointer sets the last physical address of the buffer. Whenever the PNTR register increments up to this END value the address programmed into the START register is automatically written into the PNTR register for the DMA to continue with a new sample buffer in memory.

A Sound Buffer Interrupt (SIRQ) signal is generated when the reload operation occurs which is processed by IOC as a maskable interrupt (IRQ) source.

MEMC also includes a sound channel enable/disable signal. Because this enable/disable control signal is not synchronised to the sound sampling, requests will normally be disabled after the waveforms which are being synthesised have been programmed to decay to zero amplitude; the last value loaded into the audio data latch in the VIDC will be output to each of the stereo image positions at the current audio sample rate.

IOC sound system hardware

IOC provides a programmed output control signal which is used to turn the internal speaker on or off, as well as an interrupt enable/status/reset register interface for the Sound Start Buffer reload signal generated by MEMC.

The internal speaker may be muted by the control line SMUTE which is driven from the IOC output C5. On reset this signal will be taken high and the internal speaker will be muted.

The stereo output to the headphones socket is not muted by SMUTE and will always reflect the current output of the DAC channels.

Video system

The video connector is a 15-way miniature D-type whose pin allocation is very similar to a standard VGA pin-out but with several enhancements, as detailed below:

- Pin 9 (normally used for keying) is used to supply +5V, specifically for powering an external UHF modulator. The output is protected by a 750mA fuse.
- Pin 12 provides +12V (source impedance = 1k5Ω). This output is used to provide a SCART *function switching* signal for use with SCART TVs.
- Pin 15 is an input, ID3, which may be used in the future to identify standard monitor types.

The monitor types listed below are supported. A scheme of automatically sensing the monitor type connected to the computer is implemented (see *Appendix A – Monitor adaptor cables*). This scheme ensures that a user sees a picture regardless of what monitor type is connected to the computer and that, where possible, the complete list of modes available for the particular monitor type is made available.

Monitor type		Modes
0	TV frequency/SCART TV/UHF modulator	0-17, 24, 33-36
1	Multifrequency monitor	0-21, 24-31, 33-46
3	VGA monitor	0-15, 25-28, 41-46
4	VGA/Super VGA monitor	0-15, 25-31, 41-46
5	LCD panel	0-17, 24-28
Auto	Auto-configure	Monitor-dependent

The automatic sensing scheme uses the four ID bit inputs, ID[3:0], present on the video connector to detect the type of monitor connected to the computer. The ID bits are read directly by software, where data bits D[3:0] correspond to ID[3:0]. Monitors designed for use with IBM PCs and compatibles use a coding system whereby ID[3:0] define the monitor type. ID bits are either connected to 0V or are left open circuit in the monitor or monitor cable. For example, a mono VGA monitor connects ID1 to 0V, leaving ID0 and ID2 open circuit. This ID system has been adopted and extended as detailed in the following table:

Monitor type	ID settings			
	D3	D2	D1	D0
LCD	*	1	1	1
Mono VGA	*	1	0	1
Colour VGA	*	1	1	0
Colour SVGA	*	0	1	0
Multifrequency (using composite syncs)	*	HSYNC	1	1
TV/UHF mod./ SCART	*	1	1	HSYNC

* - undefined HSYNC - horizontal sync pulse

NOTE 1: If none of the ID bits are connected to 0V or HSYNC, then the software will default to LCD.

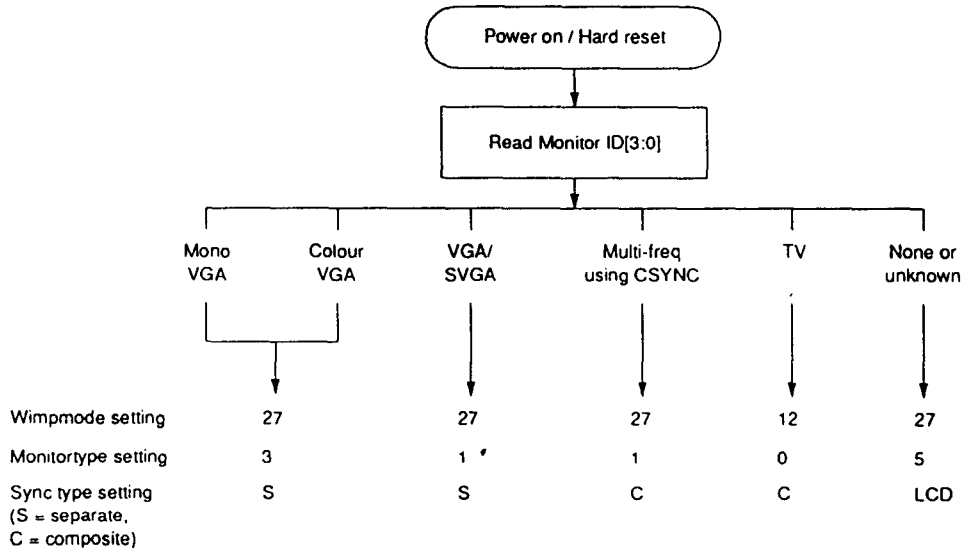
NOTE 2: the HSYNC to ID bit connections are Acorn defined and are made in the monitor cable.

The *Configure options: MONITORTYPE, SYNC and WIMPMODE have an AUTO setting (e.g. *Configure MONITORTYPE AUTO) which determines the operation of the automatic monitor type sensing scheme. At power-on or following a hard reset with all three options set to AUTO the software senses the monitor type connected and sets the Wimpmode, Sync type and Monitor type (which defines the list of available modes) for the particular monitor – see *Figure 1.8*. These are temporary values which are not written back to CMOS RAM. Subsequent *Configure Monitortype, Sync and WimpModes selected by the user overwrite the relevant AUTO setting in CMOS RAM so that the machine is initialised in the mode etc. desired – the power-on/reset sequence is the same as described above, except software uses the options selected by the user instead of the AUTO setting.

Many multi-frequency monitors have their ID bits set to Super VGA. As these are becoming more common than SVGA monitors the automatic sensing system allows multi-frequency modes whenever an SVGA monitor is detected. For those users who wish to use a genuine SVGA monitor, the system can be manually configured to SVGA using the !Configure application which overrides the automatic system. Some multi-frequency monitors have their ID bits set to VGA. Once again, use !Configure, this time to gain access to multi-frequency modes.

Appendix A – Monitor adaptor cables contains details of how to acquire cable adaptors to connect monitors that do not have a 15-way VGA connector. These adaptors take advantage of the automatic sensing scheme.

Figure 1.8: Monitor sensing



LC ASIC

The LC ASIC provides a programmable interface to monochrome flat panel LCD displays, offering 16 levels of grey scale. A large range of display formats are catered for, including 320x200 and 640x200 single panel displays, and 640x400 and 640x480 dual panel displays.

The device accepts pixel data, and horizontal and vertical sync signals, from a conventional CRT display controller. It re-times the image and converts it to greyscales, for display on an LCD panel. When used to control a dual panel display, one or two external DRAMs are needed to act as a half frame buffer. The LC ASIC supports a wide variety of DRAMs, though in most applications two 64Kx4 devices are sufficient.

Figure 1.9 is a block diagram of the LC ASIC. The LCCLK block generates clocks for the LC ASIC and the display controller, and includes a crystal oscillator. The LCVINT block synchronises the incoming video data and sync signals, and inverts the incoming data before performing a logical-to-physical colour translation. It does this by looking up the logical colour on the 16 entry on-chip palette. The LCREG block contains all the software programmable control bits in the device, and outputs them to other parts of the chip. The LCGS block converts the post-palette data to greyscales, and outputs the data to the LCDRAM block. This block stores data temporarily in the external DRAM devices, generating all necessary timing and control signals for them, and also outputs the data to the LCD panel with the correct timing. The LCCTL block generates all the internal control signals. The greyscaling system is the subject of Acorn patent application GB2245743A.

Memory system

The memory system consists of banks of DRAM directly driven by MEMC, which provides all the necessary signals and refresh operations.

MEMC uses fast page mode DRAM accesses to maximise memory bandwidth. Once the row address has been strobed into the DRAM, any column in that row may be accessed merely by strobing in the new column address. This method is used whenever a number of sequential addresses in the DRAM are to be accessed, either by the processor or during a DMA operation. The first memory access in the sequence is a non-sequential memory cycle (N cycle) where both the row and column addresses are strobed into the DRAMs. Subsequent memory accesses are sequential memory cycles (S cycles) where the previous row address is held, and only the column address is strobed into the DRAMs. The memory system runs at 12MHz and either 70ns or 80ns DRAMS are used (depending on different manufacturers' timing parameters).

The memory size is configurable for either 1MB, 2MB or 4MB by fitting the appropriate type of DRAMs to the main PCB and setting the DRAM size switches.

The base 1MB machine is two SOJ DRAMs (256Kx16).

The second MB is two 40-pin ZIPs (256Kx16).

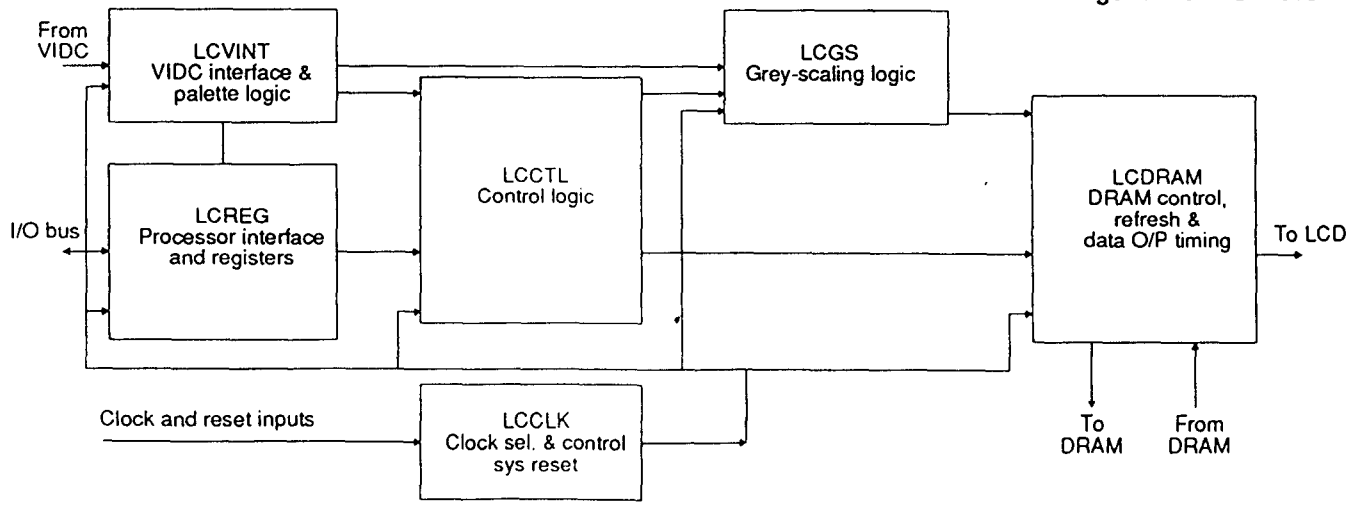
The upgrade from 2MB to 4MB uses four 28-pin ZIPs (512Kx8).

Mem size	D[31:.24]	D[23.:16]	D[15:.8]	D[7.:0]
1MB base	IC37		IC29	
2MB	IC30		IC39	
4MB	IC27	IC19	IC18	IC21

The table below shows the internal switch settings for different memory sizes.

Mem size	SW1	SW2
1MB	1-4	1-3
2MB	1-2	1-3
4MB	1-3	1-2

Figure 1.9: LC ASIC



Keyboard and mouse

The keyboard assembly comprises a keyswitch panel connected to a micro-controller on the main PCB, which serialises the keyboard and mouse data; connection to the ARM is made via a serial link to the IOC. The ARM reads and writes to the KART registers in the IOC. The protocol is essentially half duplex, so in normal operation the keyboard micro-controller will not send a second byte until it has received an ACK. The only exception to this is during the reset protocol used to synchronise the handshaking, where each side is expecting specific responses from the other and will not respond further until it has these.

In addition to this simple handshaking system, the keyboard micro-controller will not send mouse data unless specifically allowed to, as indicated by ACK MOUSE, which allows the transmission of one set of accumulated mouse coordinate changes, or the next move made by the mouse. While it is not allowed to send mouse changes, the keyboard will buffer mouse changes.

A similar handshake exists on key changes, transmitted as key up and key down, and enabled by ACK SCAN. At the end of a keyboard packet (two bytes) the operating system will perform an ACK SCAN as there is no protocol for re-enabling later. Mouse data may be requested later by means of Request Mouse Position (RQMP).

Key codes

The keyboard micro-controller identifies each key by its row and column address in the keyboard matrix and converts it to the standard row and column codes for RISC OS computers.

Row and column codes are appended to the key up or down prefix to form the complete key code.

For example, Q key down – the complete row code is 11000010 (&C2) and the column code is 11000111 (&C7).

Note: The CTRL key has N-key rollover. The Shift function has N-key rollover, but the Shift keys are not uniquely identifiable. The operating system is responsible for implementing two-key rollover, therefore the keyboard controller transmits all key changes (when enabled). The keyboard does not operate any auto-repeat; only one down code is sent, at the start of the key down period.

FN mode

The keyboard micro-controller detects the FN key down and converts those keyswitches which have legends for keys not physically present on the smaller Acorn A4 keyboard into the appropriate matrix position codes.

In addition, mouse movement and buttons are simulated by the micro-controller if cursor keys and/or Q,W,E are pressed while FN is held down.

The FN key down event is also transmitted. Various FN modes can be locked by the micro-controller.

Data protocol

Data transmissions from the keyboard are either one or two bytes in length. Each byte sent by the keyboard is individually acknowledged. The keyboard will not transmit a byte until the previous byte has been acknowledged, unless it is the HRST (HardReSeT) code indicating that a power on or user reset occurred or that a protocol error occurred; see paragraph below.

Reset protocol program

```
START reset
ONerror Send HRST code to ARM then wait for code from ARM.
IF code = HRST THEN restart ELSE error
ONrestart   clear mouse position counters
            set mouse mode to data only in response to an RMPS request.
            stop key matrix scanning and set key flags to up
            send HRST code to ARM
Wait for next code
IF code = RAK1 THEN send RAK1 to ARM    ELSE   error
Wait for next code
IF code = RAK2 THEN send RAK2 to ARM    ELSE   error
Wait for next code
IF code = SMAK THEN mouse mode to send if not zero and enable key scan
ELSE  IF code = SACK THEN enable key scanning
ELSE  IF code = MACK THEN set mouse mode to send when not zero
ELSE  IF code = NACK THEN do nothing    ELSE   error
END reset

Reset sequencing
Direction   Code        Expected    Action on   Action on   Action if
                        reply       wrong reply timeout     unexpected
                                    (Sender)    (Sender)    (Receiver)

ARM -> Kb   Hard reset  Hard reset  Resend      Resend      Hard reset
Kb  -> ARM  Hard reset  Reset Ack 1 Resend      Nothing     Hard reset
ARM -> Kb   Reset Ack 1 Reset Ack 1 Hard reset  Hard reset  Hard reset
Kb  -> ARM  Reset Ack 1 Reset Ack 2 Nothing     Nothing     Hard reset
ARM -> Kb   Reset Ack 2 Reset Ack 2 Hard reset  Hard reset  Hard reset
```

Reset protocol

The keyboard restarts when it receives an HRST code from the ARM. To initiate a restart the keyboard sends an HRST code to the ARM, which will then send back HRST to command a restart.

The keyboard sends HRST to the ARM if

- a power-on reset occurs
- a user reset occurs
- a protocol error is detected.

After sending HRST, the keyboard waits for an HRST code. Any non-HRST code received causes the keyboard to resend HRST. The pseudo program on the previous page illustrates the reset sequence or protocol.

Note: the on/off state of the keyboard LEDs does not change across a reset event, hence the LED state is not defined at power on. The ARM is always responsible for selecting the LED status. After the reset sequence, key scanning is only enabled if a scan enable acknowledged (SACK or SMAK) was received from the ARM.

Data transmission

When enabled for scanning, the keyboard controller informs the ARM of any new key down or new key up by sending a two byte code incorporating the key row and column addresses. The first byte gives the row and is acknowledged by a byte acknowledge (BACK) code from the ARM. If BACK is not the acknowledge code then the error process (ON error) is entered. When the BACK code is received, the keyboard controller sends the column information and waits for an acknowledge.

If either a NACK, SACK, MACK or SMAK acknowledge code is received, the keyboard controller continues by processing the ACK type and selecting the mouse and scan modes implied. If the character received as the second byte acknowledge is not one of NACK, MACK, SACK or SMAK, then the error process is entered.

Mouse data

Mouse data is sent by the keyboard controller if requested by an RQMP request from the ARM, or if a SMAK or MACK has enabled transmission of non-zero values. Two bytes are used for mouse position data. Byte one encodes the accumulated movement along the X axis, while byte two gives Y axis movement.

Both X and Y counts are transferred to temporary registers when data transmission is triggered, so that accumulation of further mouse movement can occur. The X and Y counters are cleared upon each transfer to the transmit holding registers. Therefore, the count values are relative to the last values sent. The ARM acknowledges the first byte (Xcount) with a BACK code and the second byte (Ycount) with any of NACK/MACK/SACK/SMAK. A protocol failure causes the keyboard controller to enter the error process (ON error).

When transmission of non-zero mouse data is enabled, the keyboard controller gives key data transmission priority over mouse data except when the mouse counter over/underflows.

Table 1.7: Code values

Mnemonic	msb	lsb	Comments
HRST	1111	1111	1-byte command,-keyboard reset.
RAK1	1111	1110	1-byte response in reset protocol.
RAK2	1111	1101	1-byte response in reset protocol.
RQPD	0100	xxxx†	1-byte from ARM, encodes four bits of data.
PDAT	1110	xxxx	1-byte from keyboard, echoes four data bits of RQPD.
RQID	0010	0000	1-byte ARM request for keyboard ID.
KBID	10xx	xxxx	1-byte from keyboard encoding keyboard ID.
KDDA	1100	xxxx	New key down data. Encoded Row (first byte) and column (second byte) numbers.
KUDA	1101	xxxx	Encoded Row (first byte) and column (second byte) numbers for a new key up.
RQMP	0010	0010	1-byte ARM request for mouse data.
MDAT	0xxx	xxxx	Encoded mouse count, X (byte1) then Y (byte2). Only from ARM to keyboard.
BACK	0011	1111	ACK for first keyboard data byte pair.
NACK	0011	0000	Last data byte ACK, selects scan/mouse mode.
SACK	0011	0001	Last data byte ACK.
MACK	0011	0010	Last data byte ACK.
SMAK	0011	0011	Last data byte ACK.
LEDS	0000	0xxx	bit flag to turn LED(s) on/off.
PRST	0010	0001	From ARM, 1-byte command, does nothing.
AMAC	0101	0xxx	Set mouse acceleration rate, encoded.
SDFN	0110	10df	d - Select/deselect PC-direct mode. f - Select/deselect FN mode processing (1=select)

† x is a data bit in the Code; e.g. xxxx is a four bit data field

Acknowledge codes

There are seven acknowledge codes which may be sent by the ARM. RAK1 and RAK2 are used during the reset sequence. BACK is the acknowledge to the first byte of a 2-byte keyboard data set. The four remaining types, NACK/MACK/SACK and SMAK, acknowledge the final byte of a data set. NACK disables key scanning and therefore key up/down data transmission as well as setting the mouse mode to send data only on RQMP request. SACK enables key scanning and key data transmission but disables unsolicited mouse data. MACK disables key scanning and key data transmission and enables the transmission of mouse count values if either X or Y counts are non-zero. SMAK enables key scanning and both key and mouse data transmission. It combines the enable function of SACK and MACK.

While key scanning is suspended (after NACK or MACK) any new key depression is ignored and will not result in a key down transmission unless the key remains down after scanning resumes following a SACK or SMAK. Similarly, a key release is ignored while scanning is off.

Commands may be received at any time. Therefore, commands can be interleaved with acknowledge replies from the ARM, for example keyboard sends KDDA (first byte), keyboard receives command, keyboard receives BACK, keyboard sends KDDA (second byte), keyboard receives command, keyboard receives SMAK. If the HRST command is received the keyboard immediately enters the restart sequence. The LEDS and PRST commands are normally acted on immediately. Commands which require a response are held pending until the current data protocol is complete. Repeated commands only require a single response from the keyboard.

Table 1.8: ARM commands

Mnemonic	Function
HRST	Reset keyboard.
LEDS	Turns keyboard LEDs on/off. A three bit field indicates which state the LEDs should be in. Logic 1 is ON, logic 0 (zero) OFF. D0 controls CAPS LOCK D1 controls NUM LOCK D2 controls SCROLL LOCK
RQMP	Request mouse position (X,Y counts).
RQID	Request keyboard identification code. The computer is manufactured with a 6-bit code to identify the keyboard type to the ARM. Upon receipt of RQID the keyboard controller transmits KBID to the ARM.
PRST	Reserved for future use, the keyboard controller currently ignores this command.
RQPD	For future use. The keyboard controller will encode the four data bits into the PDAT code data field and then send PDAT to the ARM.
AMAC	Sets acceleration rate for FN mode simulated mouse movement.
SDFN	Allows FN mode processing to be disabled and allows PC keycode conversions disabled (see *External keyboards* below).

External keyboards

The keyboard micro-controller is also connected to a PS/2-compatible 6-pin mini-DIN keyboard socket.

Periodically (about every 2s) it will check for the presence of an external PS/2 type keyboard. It does this by sending out an ECHO command and testing for a valid response. If such a response is received, the micro-controller will take keyswitch data from the external keyboard in preference to the internal keyswitch matrix. All keyswitch codes from the external keyboard are converted to RISC OS-compatible codes. LED updates from the ARM system are translated and passed onto the external keyboard. The auto-repeat function of a PS/2 keyboard is disabled by the micro-controller.

If communication with the external keyboard fails for any reason (e.g. if it is unplugged) the micro-controller will resume scanning of the internal matrix.

The conversion of PS/2 keyboard keyswitch codes into RISC OS keyboard codes can be disabled with the SDFN command. When this command is issued, data sent by the ARM processor will be passed unmodified to the external PS/2 keyboard and vice-versa. An external PS/2 keyboard does not affect mouse operation.

The micro-controller is capable of detecting whether the external keyboard is a PS/2 keyboard or an Archimedes-type keyboard, although Archimedes keyboards are not currently supported. If it is an Archimedes keyboard, it switches to a bit copy mode – it becomes a bi-directional buffer passing on the bit-stream from IOC to the external Archimedes keyboard and vice-versa. If the external Archimedes keyboard is unplugged, the micro-controller detects this and returns to normal operation. While an Archimedes keyboard is plugged in, the micro-controller can no longer monitor the mouse. Instead, the mouse must be plugged into the Archimedes keyboard. In addition, the RESET switch on the Archimedes keyboard will NOT function.

Mouse interface

The mouse interface has three switch sense inputs and two quadrature encoded movement signals for each of the X axis and Y axis directions. Mouse key operations are debounced and then reported to the ARM using the Acorn key up / key down protocol. The mouse keys are allocated unused row and column codes within the main key matrix.

Switch 1 (left)	Row code - 7	Column code - 0
Switch 2 (middle)	Row code - 7	Column code - 1
Switch 3 (right)	Row code - 7	Column code - 2

For example, switch 1 release would give 11010111 (&D7) as the complete row code, followed by 11010000 (&D0) for the column code.

Note: Mouse keys are disabled by NACK and MACK acknowledge codes, and are only enabled by SACK and SMAK codes, i.e. they behave in the same way as the keyboard keys.

The mouse is powered from the computer 5V supply and may consume up to 80mA.

Movement signals

Each axis of movement is independently encoded in two quadrature signals. The two signals are labelled REFerence and DIRection (eg X REF and X DIR). *Table 1.10* defines the absolute direction of movement. Circuitry in the keyboard decodes the quadrature signals and maintains a signed 7-bit count for each axis of mouse movement.

When count overflow or underflow occurs on either axis, both X and Y axis counts lock and ignore further mouse movement until the current data has been sent to the ARM.

Table 1.10: Direction of movement

Initial state		Next state		
REF	DIR	REF	DIR	
1	1	1	0	
1	0	0	0	Increase count by one
0	0	0	1	for each change of state.
0	1	1	1	
1	1	0	1	
0	1	0	0	Decrease count by one
0	0	1	0	for each change of state.
1	0	1	1	

Overflow occurs when a counter holds its maximum positive count (0111111 binary). Underflow occurs when a counter holds its maximum negative count (1000000 binary).

Table 1.9: Base keyswitch mapping

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	Esc	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	Print	Scroll Lock	Break
1	~	1	2	3	4	5	6	7	8	9	0	-	=	£	←	Insert
2	Home	PgUp	Num Lock	NK /	NK *	NK #	Tab	Q	W	E	R	T	Y	U	I	O
3	P	[	]	\	Del	Copy End	PgDn	NK 7	NK 8	NK 9	NK -	LHS Ctrl	A	S	D	F
4	G	H	J	K	L	;	'	Return	NK 4	NK 5	NK 6	NK +	LHS Shift		Z	X
5	C	V	B	N	M	,	.	/	RHS Shift	↑	NK 1	NK 2	NK 3	Caps Lock	LHS Alt	Space
6	RHS Alt	RHS Ctrl	←	↓	→	NK 0	NK .	NK Enter								
7	SW1	SW2	SW3											◐	■	FN

Notes:

Items in bold occur in FN mode, or when pressed in conjunction with the FN key.

NK numeric keypad
LHS lefthand side
RHS righthand side

Floppy disc drive

The floppy disc drive fitted to the computer supports both 3.5 inch double-sided double-density and 3.5 inch double-sided high-density floppy discs.

Pin assignment:

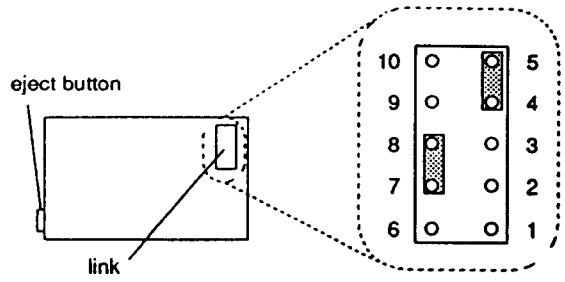
Pin	Signal	Pin	Signal
1,3,5	+5V	11	HD IN
2	INDEX	12	$\overline{\text{DIR}}$
4	SEL	14	$\overline{\text{STEP}}$
6	DISC CHANGE	16	$\overline{\text{WRITE DATA}}$
8,13,15,17, 19,21,23,25	0V	18	$\overline{\text{WRITE GATE}}$
7	N/C	20	$\overline{\text{TRACK 0}}$
9	$\overline{\text{HD OUT}}$	22	$\overline{\text{WRITE PROTECT}}$
10	MOTOR ON	24	$\overline{\text{READ DATA}}$
		26	$\overline{\text{SIDE 1}}$

Performance

Item	Specification
Drive type	SMD-1040-321 (Epson)
Capacity	1MB/2MB (unformatted)
Transfer rate	500/250Kbs^{-1}
Track density	135TPI
No. tracks/disc (double-sided)	160
Track to track step rate	3ms
Seek settle time	15ms
Power supply	+5Vdc (± 5%)
Maximum continuous power (typical)	3W
Disc life	3x10^6 passes/track @ 300rpm
Average seek time	95ms
Average latency	100ms
Error rates	1 in 10^9 recoverable read errors 1 in 10^{12} non-recoverable read errors 1 in 10^6 seek errors
MTBF	15,000 POH, 12.5% spindle motor duty cycle
I/P signal levels	
Logic 0	0.4V max
Logic 1	2.5V min
O/P signal levels 1KΩ load to +5V	
Logic 0	0.4V max
Logic 1	2.4V min to 5.25V max

Link settings

The floppy disc drive has a cut-out in its casing, through which you can see a link. The jumpers should be set to the "MODE 1" positions as follows:



Drive input signals

$\overline{\text{MODE SELECT}}$

Logic 0 (pin 11): 1MB mode. Logic 1: 2MB mode.

$\overline{\text{DRIVE SELECT}}$ [0:1]

These signals condition all drive interface signals except $\overline{\text{MOTOR ON}}$ (which is independent of $\overline{\text{DRIVE SELECT}}$). The drive will only respond to an interface signal when the relevant $\overline{\text{DRIVE SELECT}}$ signal is active. The drive select switch (if fitted) on the drive is set to Drive 0.

MOTOR ON

Spindle motor rotates when $\overline{\text{MOTOR ON}}$ is active AND a disc has been inserted in the drive.

DIRIN

Logic 0: a $\overline{\text{STEP}}$ pulse causes the head to be stepped in towards the spindle. Logic 1: a $\overline{\text{STEP}}$ pulse causes the head to be stepped away from the spindle.

STEP

A $\overline{\text{STEP}}$ pulse causes the head to be stepped in or out one track, depending on the polarity of $\overline{\text{DIRIN}}$. Stepping to negative tracks is inhibited by the drive.

WRITE DATA

MFM data written to the disc. The drive gates this signal with $\overline{\text{WRITE ENABLE}}$.

$\overline{\text{WRITE ENABLE}}$

Logic 0 enables the current drive's write head. The drive delays side switching and head stepping until the internal trim erase process is completed.

SIDE 1

Logic 0 selects the upper head, logic 1 the lower head.

Drive output signals

$\overline{\text{INDEX}}$

Index pulses are generated by the drive when the drive is Selected and the drive is ready.

TRACK 0

This signal is logic 0 when the head is positioned over track 0 as determined by the track 0 sensor (with or without a disc inserted).

WRITE PROTECT

Logic 0 indicates that a write protected disc is inserted.

READ DATA

MFM data read from the disc.

DISC CHANGE

This signal indicates to the system when a disc has been removed from the drive. Logic 0: at power-on and when the disc is removed from the drive. Reset to logic 1 by a STEP pulse when a disc is inserted and the drive is selected.

Operation of interface

Hardware

The floppy disc section of the 711 controller comprises a 765 floppy disc controller, which is widely used in IBM PCs (and compatibles).

There are several differences in operation between the 711-based interface and the interface based around the 1772 floppy disc controller (used in older Archimedes machines).

In common with the PC-AT interface the drive's READY signal is not used. This signal was available on older floppy drives but the majority of modern drives (and future 4MB ones) do not provide a READY signal. Instead the drive INDEX signal is fed directly to IOC and the software uses this signal together with suitable time delays to determine when the drive is ready. In this way there is a common method of determining when a drive is ready for all types of drive.

The hardware provides a MOTOR ON signal.

The maximum sink current of the floppy interface is 48mA. A single 3.5" drive requires the floppy disc controller to typically sink 5mA.

The 711 supports both MFM and FM recording. Older Acorn formats (as well as IBM formats) can be read, written and formatted as listed below. In addition, a new 1.6Mbyte ADFS F format is supported at a data rate of 500kbs^{-1}. This format has 10 x 1024 byte sectors per track (each side) with a 1 sector skew between both surfaces of the disc.

Formats supported

- ADFS F, MFM 500KHz (read/write/format)
- ADFS L, D and E, MFM 250kHz, (read/write/format)
- BBC Master 128 ADFS S and M, MFM 250kHz (read/write)
- DFS, FM 125kHz (requires a DFSReader utility to read/write)

Two features of the 765 floppy disc controller are:

- it cannot format a disc without an INDEX Address field following the physical INDEX pulse
- the skew between top and bottom sides of a disc must be an integral number of sectors.

Discs formatted on a 711 based machine are therefore not physically identical to those produced on a 1772 base machine. However, this does NOT affect interchangability between 711 and 1772-based machines. The leading Index address field feature causes discs formatted as ADFS L format (16 x 256 byte sectors/track) to have rather reduced inter-sector gaps and thus be susceptible to drive speed variation beyond ±1.5%. This is only likely to be a problem when interchanging ADFS L format discs between poor quality disc drives.

Software

The new RISC OS driver supports the MultiFS specification, thereby allowing RISC OS to read/write discs in a hardware-independent manner from virtually any computer system supporting IBM/ISO compatible disc formats.

In keeping with the original 1772 driver software, it is possible to *Configure step rates of 2, 3, 6 or 12ms on a drive-by-drive basis. However, the step rates provided by the 765 controller depend on the data clock rate selected and it is not always possible to set exactly the step rate configured. Note that in single and double density modes selection of the 12ms step rate actually results in a 26ms rate being used. The following table shows the configured and actual step rates used for various data clock rates (in kbs^{-1}):

Configured step rate (ms)	Actual step rate (ms)			
	125 (kbs^{-1})	250 (kbs^{-1})	300 (kbs^{-1})	500 (kbs^{-1})
2	2	2	1.7	2
3	4	4	3.3	3
6	6	6	6.7	6
12	26	26	25	12

Hard disc drive

The hard disc drive used on the computer is a 2.5 inch IDE (Intelligent Drive Electronics) drive and has the following typical performance parameters:

Capacity	60MB
Power supply	+5V
Ave. seek time	25ms max
Start/stop cycles	40,000 min
Spin up after auto spin down	10s typical (20s max)
Stop time	5s max
MTBF	50,000 POH
Error rates	< 1 in 10^{10} recoverable read errors < 1 in 10^{13} non-recov. read errors < 1 in 10^{6} seek errors
Power consumption:	
read/write	2.5W max
idle	1.5W max
spin-up	-
standby	0.4W max
sleep	0.25W max

This type of drive is used increasingly in PC-AT computers and an official standard describing the hardware and software interface has recently been agreed by the CAM (the Common Access Method) Committee. The hard disc controller of an IDE drive is integrated into the circuit board of the drive so that the interface to the computer is very simple:.

Pin	Signal	Dir.	Pin	Signal	Dir.
1	$\overline{\text{RESET}}$	O	23	$\overline{\text{IOW}}$	O
2	GND		24	GND	
3	DATA 7	I/O	25	$\overline{\text{IOR}}$	O
4	DATA 8	I/O	26	GND	
5	DATA 6	I/O	27	$\overline{\text{IORDY}}$	I
6	DATA 9	I/O	28	N/C	
7	DATA 5	I/O	29	N/C	
8	DATA 10	I/O	30	GND	
9	DATA 4	I/O	31	IRQ	I
10	DATA 11	I/O	32	$\overline{\text{IO16}}$	I
11	DATA 3	I/O	33	HOST A1	O
12	DATA 12	I/O	34	$\overline{\text{PDIAG}}$	I/O
13	DATA 2	I/O	35	HOST A0	O
14	DATA 13	I/O	36	HOST A2	O
15	DATA 1	I/O	37	$\overline{\text{HOST CS0}}$	O
16	DATA 14	I/O	38	$\overline{\text{HOST CS1}}$	O
17	DATA 0	I/O	39	$\overline{\text{IN USE LED}}$	I
18	DATA 15	I/O	40	GND	
19	GND		41	+5V	
20	KEY		42	+5V	
21	N/C		43	GND	
22	GND		44	$\overline{\text{AT/XT}}$	

The IDE interface can support one drive which is known as the Master. Like SCSI, the IDE interface is a logic level interface. Drives accept high level commands (e.g. Read Sector) and generate an interrupt on completion of a command. Being intelligent, IDE drives possess features which result in faster operation and more efficient storage of data. For example, many have a buffer memory which they use to cache several sectors of data during reads and writes. They also invariably perform logical to physical sector translation and so can take advantage of recording techniques (e.g. zoned recording).

The IDE interface is essentially an extension of the computer's internal data, address and control buses. Because of this, the cable length is kept to a minimum.

The RISC OS IDE driver software adheres as closely as possible to the CAM recommendations. It does not implement any of the Multiple commands which allow multiple sector operations with a single interrupt since many drives do not as yet support these commands. Disc transfers are performed one sector/interrupt with individual sectors being transferred to/from disc at a rate of approx. 2.4MBs^{-1}. *Figure 1.10* on page 1-21 shows a sector write to disc (using a VGA monitor in mode 27).

Continuous large file transfer rates of 500 to 700kbs^{-1} can be sustained in all screen modes.

There is no separate filing system for the IDE drive. It is assigned an ADFS drive number (usually 4).

Econet (optional network connection)

The A4 Econet interface module (ALA66) is based on the existing Econet II (ADF10) design. It is a repackaged design using surface mount technology and incorporates additional circuitry for providing a power down feature.

Econet General

Econet is a low cost synchronous differential clock and data communication channel. Each station has an interface based on the 68B54 Advanced Data Link controller. This is an intelligent peripheral device used to transmit and receive data packets over the communications channel between two or more computers using a Bit Orientated Protocol. The ADLC converts parallel to serial data and constructs the packets sent over the network. Its functions include automatic generation of opening and closing flags, Cyclic Redundancy Check calculations/checking and zero insertions and deletions.

The 68B54 drives the channel using differential line drivers. High speed comparators and monostable elements provide the receive/collision detect function.

Power save circuitry

An extra signal on the computer interface $\overline{\text{ECON}}$ is asserted by the computer when the network is not required. This disables a set of buffers between the computer interface and the 68B54. It also removes power from the 68B54 and the rest of the Econet circuitry via a transistor switch.

Parallel port

The parallel port is an IBM PC-XT/AT compatible port and also has a PS/2 like bi-directional capability. It can be configured via software for output only (printer application) or input/output (e.g. scanner application).

Connector: 25 way D (Female on the computer)

Pin	Signal	Direction/ Type
1	/STROBE	O
2	DATA 0	I/O
3	DATA 1	I/O
4	DATA 2	I/O
5	DATA 3	I/O
6	DATA 4	I/O
7	DATA 5	I/O
8	DATA 6	I/O
9	DATA 7	I/O
10	/ACK	I
11	BUSY	I
12	PE	I
13	SLCT	O
14	/AUTOFD XT	O
15	/ERROR	I
16	/INIT	O
17	/SLCT IN	O
18 to 25	GND	

The data bus is capable of sinking 24mA and the control signals ($\overline{\text{STROBE}}$, $\overline{\text{SLCTIN}}$, $\overline{\text{INIT}}$ and $\overline{\text{AUTOFD}}$) are open collector capable of sinking 24mA. These control signals are driven in both input and output mode whilst the control signals $\overline{\text{ACK}}$, BUSY, PE, SLCT and $\overline{\text{ERROR}}$ are always input signals.

Many printers work with a subset of the signals available, for example: STROBE, ACK, BUSY and the 8 data lines.

Base address for the PC I/O system is 3010000H. The offset into this area for the printer port is 4* 278H = 9E0H

Therefore the printer port base address is 30109E0H.

The printer port has three registers:

Data Latch:
Printer Base address + 4 * 00H = 30109E0H

Status Register:
Printer Base address + 4 * 01H = 30109E4H

Control Register:
Printer Base address + 4 * 02H = 30109E8H

Note: These addresses are for byte accesses.

Data Latch

Read / Write register for printer data. In normal mode, data written to this register is put onto the data pins to the printer. Data read from this address is the data that is on the printer port data pins.

Status Register

Read only register.

Parallel port interrupt

The Parallel port interrupt signal ($\overline{\text{PINTR}}$) generated by the 711 is not used directly. Instead it is latched in IOEB to produce the signal $\overline{\text{LPINTR}}$ which is then fed into IOC. $\overline{\text{LPINTR}}$ is latched on the rising edge of $\overline{\text{PINTR}}$ (assuming that the interrupt is programmed as active low in the 711) which corresponds to the falling edge of $\overline{\text{ACK}}$. Once latched $\overline{\text{LPINTR}}$ may be cleared by a read or write to the Printer Clear register (&3350058). *Figure 1.11* on page 1-21 shows various control signals during a print operation.

The following notes describe the printer port hardware registers and a typical use for each pin. The actual use of each signal will depend upon the operating system, application, printer driver and type of printer connected.

Bit	Signal	Meaning
Bit 7	/BUSY	This bit reflects the INVERTED state of the BUSY input pin. Note: The signal is inverted. ie Read a 0 when the pin is high. A 0 means the printer is busy and cannot accept data. A 1 means that the printer is ready to accept data.
Bit 6	/ACK	This bit reflects the state of the /ACK input pin. A 0 means that the printer has received a character and is ready to accept another. A printer would normally pulse this pin low when it is ready to receive the next character. The rising edge of this signal will latch a pending interrupt.
Bit 5	PE	Paper Empty. This bit reflects the state of the PE input. A 0 indicates the presence of paper. A 1 indicates a paper end condition.
Bit 4	SLCT	This bit reflects the state of the SLCT input pin. A 0 means the printer is not selected. A 1 means the printer is on line.
Bit 3	/ERROR	This bit reflects the state of the /ERROR input. A 0 means that an error condition has been detected. A 1 indicates no errors.
Bits 2-0	Reserved	

Figure 1.10: Sector write to disc

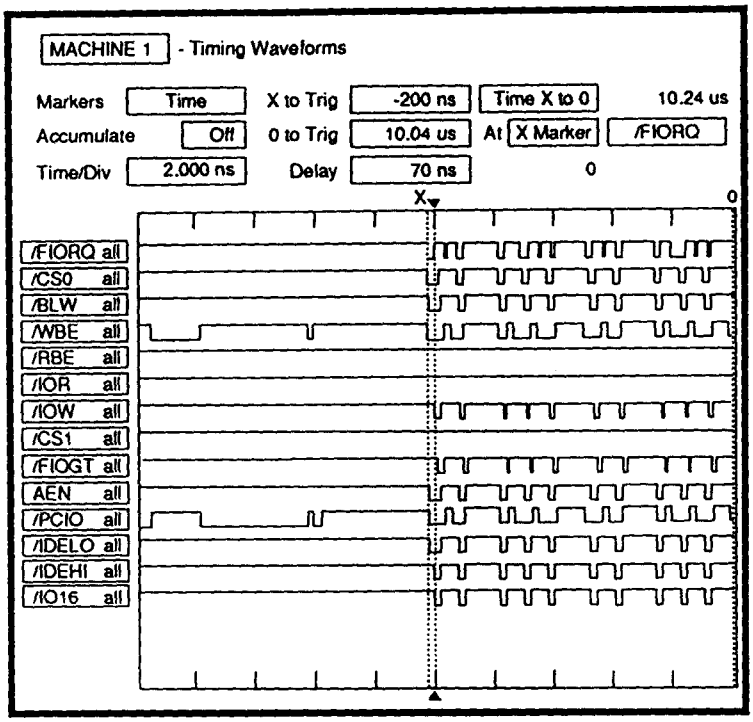
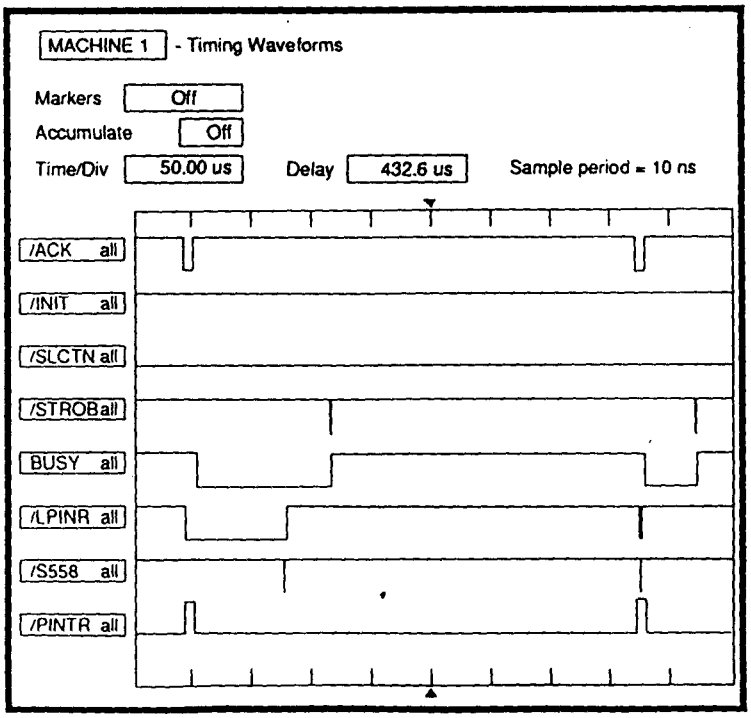


Figure 1.11: Parallel port control signals



Control Register

Read / Write register.

Bit	Signal	Meaning
Bit 7-6	Reserved	
Bit 5	DIR	Data direction. Valid only in extended mode. A 0 for output. A 1 for input. Recommendation: Write a 0 for normal use.
Bit 4	IRQEN	Used in a PC system to enable interrupts. On some Acorn systems the state of this bit is ignored. Hardware reset to 0. Recommendation: Always write a 1. Interrupt disabling should be done in IOC.
Bit 3	/SLCTIN	Used to drive the /SLCTIN output pin. A hardware reset sets the register to 0 and the pin high. A 1 selects the printer.
Bit 2	/INIT	Used to drive the /INIT output pin. A hardware reset sets the register to 0 and the pin low. A 0 initializes the printer. (Set low for 50µS minimum)
Bit 1	/AUTOFD	Used to control the /AUTOFD output pin. Note: Writing a 1 sets the pin low. A hardware reset sets the register to 0 and the pin high. A 1 causes the printer to generate a line feed after each line is printed. A 0 means no autofeed.
Bit 0	/STROBE	Used to control the /STROBE output pin. A hardware reset sets the register to 0 and the pin high. A 1 in this bit generates an active low output. For normal printing, the data should be setup at least 0.5µs before strobe.

Serial port

The serial port is controlled by the 711 which contains a NS16450 compatible UART. The serial port is an asynchronous serial interface which uses a 9-way D-type connector.

Pin	Signal
1	DCD I/P
2	RXD O/P
3	TXD O/P
4	DTR O/P
5	0V
6	DSR I/P
7	RTS O/P
8	CTS I/P
9	RI I/P

The line drivers and receivers meet all the EIA RS-232C and CCITT V.28 specifications. In particular, the line driver meets the minimum RS-232/V.28 output voltage swing of ±5V when all outputs are driving the 3K minimum allowable load impedance. The line driver's characteristics ensure reliable operation at 19200 baud provided that the load capacitance does not exceed the RS-232/V.28 recommended limit of 2500pF (i.e. several metres of cable). Operation at baud rates greater than 19200 baud (which the UART can generate as detailed below) may even be possible over short cable lengths and under light line driver loading.

The 16450 UART potentially allows all the baud rates shown in the table below to be programmed, although currently the operating system does not support the two highest baud rates.

Baud Rate	Percentage error
50	0.001
75	*
110	*
134.5	0.004
150	*
300	*
600	*
1200	*
1800	*
2000	0.005
2400	*
3600	*
4800	*
7200	*
9600	*
19200	*
38400	*
56000	0.030

* indicates 0.002% error

The UART's programmable baud rate generator uses the 711 24MHz crystal oscillator which it divides by 13 to produce a 1.8462MHz clock. This is further divided by the transmitter and receiver sections of the UART to produce the baud rate selected. The same baud rate is used for both receiving and transmitting serial data (i.e. split baud rates are not supported).

Other programmable features of the UART include:

- 5 to 8-bit character size
- 1, 1.5 or 2 stop bits
- parity options

For backwards compatibility the software interface is an extended version of that used on older RISC OS computers which use the 65C51 UART. The 711 contains two serial interfaces. The second is not used.

Power supply system

DANGER
THE POWER SUPPLY IS A SEPARATE REPLACEABLE ITEM, AND CONTAINS NO USER SERVICEABLE PARTS.
ALL ACORN POWER SUPPLIES CONTAIN HAZARDOUS VOLTAGES AND MUST NOT BE OPENED BY UNAUTHORISED PERSONNEL.
SAFETY EARTH CONTINUITY TESTING MUST BE CARRIED OUT AFTER ANY POWER SUPPLY HAS BEEN OPENED.

The power supply system for a portable computer is considerably more complex than that of a conventional desktop computer. It must capable of supplying power to the computer from either an external power adapter or the internal battery pack, switching smoothly between the two as necessary, monitoring the state of the battery pack and controlling the battery charging process whenever an external power adapter is connected.

Both the battery pack and the external power adapter supply a voltage much higher than the 5 volts required for the system logic and hence a DC/DC converter is used to produce the required system voltage.

When the external power adapter is connected the internal battery pack will be charged from a constant current source built into the external power adapter. The charging process is monitored and controlled by a single chip micro-controller (BMU) which functions independently of the main ARM CPU.

When the external power adapter in not connected power is supplied by the battery pack. The BMU monitors the discharge current and displays the calculated charge remaining in the battery on the five segment LCD 'gas-gauge'. Battery voltage is also monitored and the host system is alerted via interrupts when it drops below pre-determined thresholds.

Battery status information is passed to the ARM via the I^2C bus. Control information can also be passed from the ARM to the BMU via the I^2C bus.

WARNING!

Writing erroneous data to the BMU could cause overcharging of the battery pack and a resultant reduction in battery life. Details of the software interface to the BMU are given in the RISC OS 3 Programmer's Reference Manual.

External Power Adapter

The external power adapter converts the AC mains supply to a low voltage (typically 25V) dc supply. The regulated dc supply then splits into two separate supplies, a 21V supply (UMAIN) directly into the computer unit to the DC/DC converter (via the ON/OFF switch) and the other (UBATT) being converted into a switchable rate current source within the power adapter. The current source is used to charge the battery, with the charge rate being controlled by the BMU via control signals on the 9 pin power connector.

Circuit Description

The heart of the battery management system is an Hitachi HD404304F 4 bit micro-controller. The main features of this device are:

- 4K x 10bit program ROM
- 96 nybbles user RAM
- Two 8-bit timers
- 4 channel 8-bit a/d converter
- 16 level stack
- 5 prioritised interrupts
- Very low power 'Stop mode'.

For further details, refer to the manufacturer's datasheet.

The A/D system is used to monitor battery voltage, battery current and battery temperature. These three parameters determine the action of the BMU (Battery Management Unit). In addition to the three analogue inputs the BMU has several other digital control input and output signals:

Port	Signal	Function
R0.0	LCD20	'Gas-gauge 20%' segment drive
R0.1	LCD40	'Gas-gauge 40%' segment drive
R0.2	LCD60	'Gas-gauge 60%' segment drive
R0.3	LCD80	'Gas-gauge 80%' segment drive
R1.0	LCD100	'Gas-gauge 100%' segment drive
R1.1		Not used, connected to ground
R1.2		Not used, connected to ground
R1.3	LCDCOM	'Gas-gauge' common connection
R2.0	LIDSWITCH	Detect lid closed or open
R2.1		Not used, connected to ground
R2.2		Not used, connected to ground
R2.3		Not used, connected to ground
R3.0	RESETBLK	Prevent further reset pulses (see below)
R3.1		Not used, open circuit
R3.2	SDA	I^2C bus data (interrupt input)
R3.3	SCL	I^2C bus clock
D0	LOWBAT	Low battery warning LED drive
D1	CHARGE	Battery-on-charge LED drive
D2	SCL	I^2C bus clock
D3	SDA	I^2C bus data
D4	CRSEL1	Charge rate select
D5	CRSEL2	Charge rate select
D6	HOSTINT	Host interrupt
D7	HOSTSW	Detect state of main power switch
D8	BMUSER	Serial debug data output
D9	UMAIN	Detect presence of charger
D10	SUPP12	Switch on 12V supply for op-amps
D11	MAINON	Enable DC/DC converter
D12		Not used, open circuit

Analogue signal inputs

All three analogue signals are pre-processed by operational amplifier stages before being fed into the BMU A/D converter. All analogue inputs have an input range of 0V to Vref, where Vref (nominally 5V) is a buffered version of the BMU Vcc supply. The Vcc supply for the A/D converter is Vref, this eliminates errors due to differences between Vref and the supply.

Battery Temperature

The battery pack contains a series connected pair of positive temperature coefficient thermistors with a nominal impedance of 2KΩ at 25°C. This is fed from a high precision (0.1%) 2KΩ resistor from Vref. An op-amp provides a simple buffer to protect the BMU analogue input.

Input specification:

Input range: 0°C to 50°C
Resolution: 2°C
Accuracy: 2°C

Battery Current

Battery current maybe positive or negative depending on whether the battery is charging or discharging. A sense resistor is placed in the battery negative line, the voltage across which is amplified by an op-amp and fed to the BMU analogue input. The amplifier stage is biased to half Vref to give a mid-range reading when battery current is zero. Use of precision resistors and software self-calibration eliminates the need for any manual calibration of the circuit.

Input specification:

Input range: –1300mA to +1300mA
Resolution: 10.3mA
Accuracy: 25mA

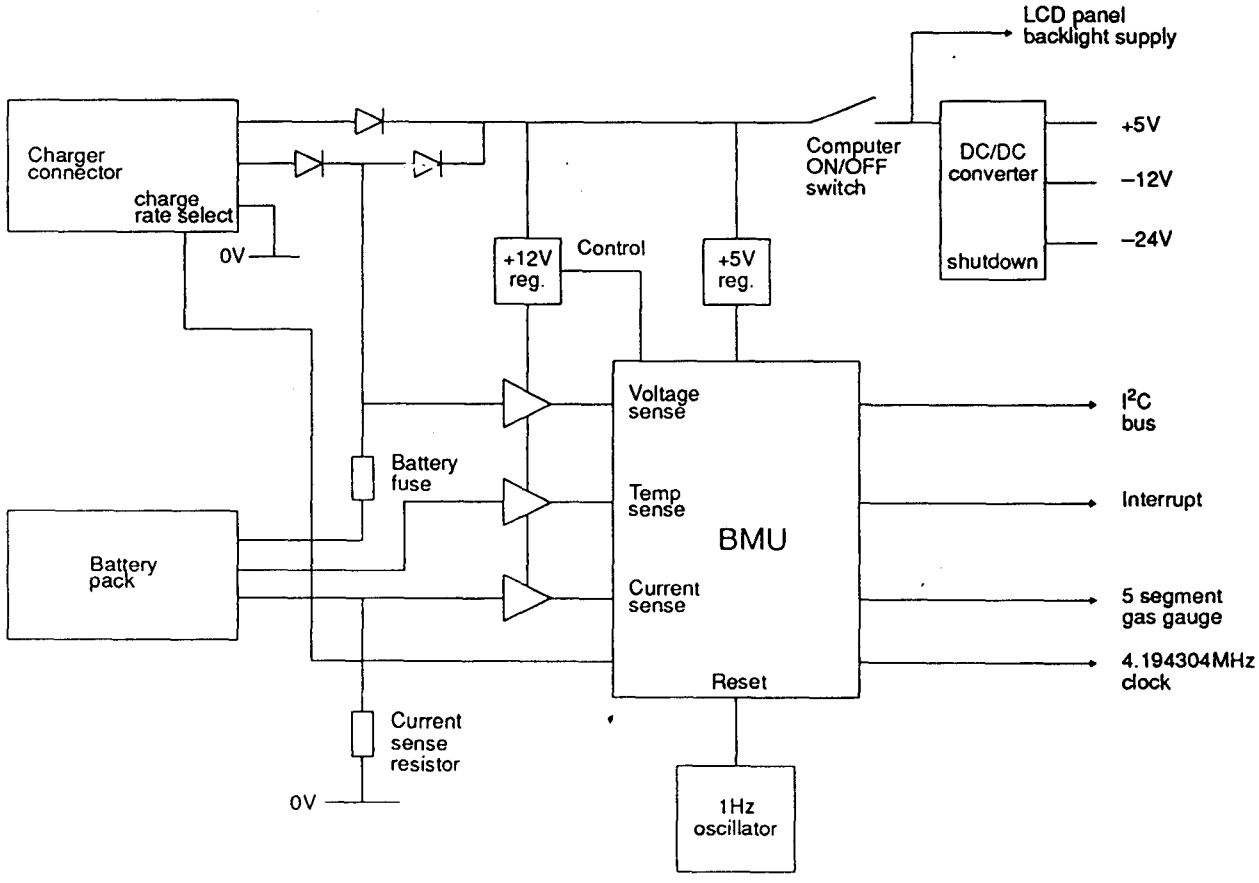
Battery Voltage

Battery voltage is fed to a high impedance potential divider. The output from the potential divider is then fed through a buffer amplifier stage to protect the BMU analogue input.

Input specification:

Input range: 0V to +25V
Resolution: 97.7mV
Accuracy: 200mV

Figure 1.12: Power control system



Digital Signals

Gas-Gauge

The 'Gas-gauge' displays the calculated charge remaining in the battery pack. It is displayed as a percentage of the nominal usable capacity of the battery pack (typically approx. 1650mAH) to a resolution of 20%. The BMU drives a square wave onto the LCD common and an out-of-phase square wave onto the input of the segment to be 'lit'. The other segments are all driven with an in-phase square wave. These square waves are generated in software with a frequency of approximately 32Hz.

Lid Switch

The lid switch causes the screen to be switched off when the lid is closed. This input is fed from a mechanical switch in the lid assembly. The signal has a pull-up resistor on it (connected to the main system 5V supply) and is pulled to 0V when the switch is closed (lid is closed). The switch is debounced in software with a debounce period of 1 second.

Reset Blocking

This active low output is used to block further reset pulses being generated by the low power 555 reset pulse generator circuit. This is achieved by pulling the reset input of the 555 low.

I^2C Bus signals

Both the I^2C data line (SDA) and the I^2C clock line (SCL) are fed to two inputs on the BMU. The D port inputs are used to provide single instruction bit tests of the state of the signals. D ports are only able to pull high so the totem pole outputs of the R3 port are used to drive the I^2C bus signals during a transmit phase of the I^2C protocol. In addition the R3.2 input is also the highest priority interrupt of the BMU system and is used to switch the BMU software into I^2C transfer processing.

CHARGE and LOW-BATTERY LED drivers

These outputs source the current for the red and green sections of the tri-colour 'low-battery' and 'on-charge' indicator LED. Colour selection and flashing is all controlled in software.

Charge rate select signals

The power adaptor used to charge the A4 battery pack provides a current source UBATT with a selectable current level. The low current level is between 60mA and 70mA (used for trickle charge) and the higher level is between 320mA and 380mA (used for quick charge). The active high charge rate select output signal CRSEL1 is used to select between the two charge rates. CRSEL1 low is trickle charge, CRSEL1 high is quick charge.

Host System Interrupt

This active low output signal is used to generate an interrupt in the host system when certain events are detected by the BMU software. An external transistor circuit generates an open-collector signal which has a pull-up resistor to the host system +5V supply.

Host Power Switch Position

When the host switch is closed this signal goes high. When the host switch is opened this signal goes low. The state of this signal is regularly scanned by the software.

Serial debug

The contents of the BMU RAM are transmitted in PPM format on this pin, compatible with the standard Acorn test adaptor system.

Charger presence

This input signal is used to detect the presence of an external charger. When a charger is plugged in (and switched on) this signal will go high.

Op-Amp 12V supply control

To keep quiescent supply current to a minimum when the BMU is in stop mode the power to the op-amps is switched off. This active high output allows the BMU to enable or disable the 12V supply.

DC/DC Converter control

To prevent erratic system behaviour when the battery voltage gets very low the BMU uses this active high output to disable the DC/DC converter (and hence disable the host system 5V supply) at a predetermined battery voltage level. This also ensures that there is sufficient potential from the battery pack to sustain proper BMU operation.

Reset Pulse Generator

The BMU is able to track the self-discharge of the battery pack whether the host system is active or not. This is necessary in order to maintain a reasonably accurate estimation of charge remaining in the battery pack and hence how much charging is required.

The micro-power 555 timer generates a 10mS active high reset pulse once each second (±10%). This reset pulse takes the BMU out of stop mode and it checks for the presence of a charger or a closed host switch. If neither if these are true then a simple self-discharge calculation is carried out and the BMU re-enters stop mode. (NB. The op-amp 12V supply is not enabled, keeping average current consumption over a one second period to less than 500µA). If a charger is present or the host switch is closed then the BMU will activate the reset-blocking signal to prevent further reset pulses, and begin tracking battery charge state.

Plugs

Plug	Fitted	Function/Specification
PL1	Yes	Serial Port. (IBM PC-AT Pinout) 9-way D-type plug Pin Signal — Pin Signal 1 DCD — 6 DSR 2 RxD — 7 RTS 3 TxD — 8 CTS 4 DTR — 9 RI 5 0V
PL2	Yes	IDE hard disc drive data connector. This is a 44-way box-header containing all the signals required by the drive in AT mode. Pin Signal — Pin Signal 1 $\overline{RST}$ — 2 0V 3 DATA7 — 4 DATA8 5 DATA6 — 6 DATA9 7 DATA5 — 8 DATA10 9 DATA4 — 10 DATA11 11 DATA3 — 12 DATA12 13 DATA2 — 14 DATA13 15 DATA1 — 16 DATA14 17 DATA0 — 18 DATA15 19 0V — 20 nc 21 nc — 22 0V 23 $\overline{IOW}$ — 24 0V 25 $\overline{IOR}$ — 26 0V 27 $\overline{IORDY}$ — 28 nc 29 nc — 30 0V 31 IRQ — 32 $\overline{IO16}$ 33 LA3 — 34 $\overline{PDIAG}$ 35 $\overline{LA2}$ — 36 $\overline{LA4}$ 37 $\overline{CS0}$ — 38 $\overline{CS1}$ 39 SLV/ACT — 40 0V 41 +5V — 42 +5V 43 0V — 44 $\overline{AT/XT}$
PL3	Yes	Econet upgrade module socket. Pin Signal — Pin Signal 1 +5V — 2 LA2 3 0V — 4 LA3 5 BD0 — 6 LA4 7 BD1 — 8 $\overline{LA5}$ 9 BD2 — 10 $\overline{WBE}$ 11 BD3 — 12 $\overline{S2}$ 13 BD4 — 14 $\overline{CLK2}$ 15 BD5 — 16 $\overline{ECON}$ 17 BD6 — 18 $\overline{S4}$ 19 $\overline{BD7}$ — 20 $\overline{PIRQ}$ 21 $\overline{RST}$ — 22 $\overline{EFIQ}$ 23 0V — 24 $\overline{PWE}$ 25 0V — 26 $\overline{PRE}$
PL4	Yes	Charge state indicator. 6-way 2mm SIL header used to provide electrical connection to the 5 segment LCD charge state indicator. Pin Signal 1 CHRGECOM 2 CHRGE20 3 CHRGE40 4 CHRGE60 5 CHRGE80 6 CHRGE100

Plugs

Plug	Fitted	Function/Specification
PL5	Yes	Battery/Switch Connector. 6-way 2mm DIL boxed header used to provide electrical connection to the the battery pack and the computer on/off switch. Pin Signal 1 USUPP 2 USUPPS 3 BATT– 4 TEMP+ 5 BATT+ 6 0V
PL6	Yes	Charger Connector. 10-way 2mm DIL boxed header used to provide electrical connection to the external charger unit. Pin Signal — Pin Signal 1 NC — 6 0V 2 UMAIN — 7 IBATT 3 UBATT — 8 0V 4 0V — 9 0V 5 CRSEL2 — 10 CRSEL1
PL7	Yes	DC/DC convertor connector. 10-way 2mm DIL straight header used to provide electrical connection to the DC/DC convertor board Pin Signal — Pin Signal 1 USUPPS — 6 MAINON 2 0V — 7 NC 3 0V — 8 M24V 4 5V — 9 NC 5 5V — 10 NC

Sockets

Skt	Fitted	Function/Specification
SK1	Yes	9-way mini-DIN providing connection for quadrature mouse.
SK2	Yes	Stereo headphone output. 3-way 3.5mm stereo jack socket providing output to "Walkman-type" 32 ohm stereo headphones. Pin Signal 1 GND (outer) 2 RIGHT (centre) 3 LEFT (tip)
SK3	Yes	LCD panel interface Connector. 20 Way 1mm Flex connector used to connect LCD panel to main PCB. Pin Signal — Pin Signal 1 LIDSWITCH — 11 LEDFLOPPY 2 SPEAKER — 12 M24V 3 LCDON — 13 5V 4 BL2 — 14 0V 5 0V — 15 NC 6 NC — 16 USUPPS 7 5V — 17 5V 8 LEDBATTLO — 18 LEDACON 9 HDLED — 19 LEDCHARGE 10 USUPPS — 20 NC
SK4	Yes	LCD panel interface Connector. 20 Way 1mm Flex connector used to connect LCD panel to main PCB. Pin Signal — Pin Signal 1 DF — 11 FLM 2 CL1 — 12 0V 3 NC — 13 0V 4 CL2 — 14 0V 5 NC — 15 LD3 6 LD2 — 16 LD1 7 LD0 — 17 UD3 8 UD2 — 18 UD1 9 UD0 — 19 5V 10 OEL — 20 5V
SK5	Yes	Floppy Disc Drive Data Connector. 26-way 1.25mm Flex connector used to connect the internal floppy disc drive to the main PCB. Pin Signal — Pin Signal 1 +5V — 2 INDEX 3 +5V — 4 SEL 5 +5V — 6 DISC CHANGE 7 nc — 8 0V 9 $\overline{\text{HD OUT}}$ — 10 $\overline{\text{MOTOR ON}}$ 11 HD IN — 12 $\overline{\text{DIR}}$ 13 0V — 14 $\overline{\text{STEP}}$ 15 0V — 16 $\overline{\text{WRITE DATA}}$ 17 0V — 18 $\overline{\text{WRITE GATE}}$ 19 0V — 20 $\overline{\text{TRACK 0}}$ 21 0V — 22 $\overline{\text{WRITE PROTECT}}$ 23 0V — 24 $\overline{\text{READ DATA}}$ 25 0V — 26 $\overline{\text{SIDE 1}}$

Sockets

Skt	Fitted	Function/Specification
SK6	Yes	RGB video socket. This is a 15-way mini D-type socket providing an interface to RGB monitors and SCART TVs. RGB video levels are 0.7V Pk-Pk into 75Ω. Sync voltage levels are >= 2.0V (TTL). Pin Signal 1 RED 2 GREEN 3 BLUE 4 ID2 5 0V 6-8 0V 9 +5V (750mA fuse) 10 0V 11 ID0 12 ID1/SCART func. switching 13 HSYNC 14 VSYNC/CSYNC 15 ID3
SK7	No	Video hybrid (internal)
SK10	Yes	Parallel printer port. 25-way D-type socket providing a parallel printer interface. Pin Signal — Pin Signal 1 $\overline{\text{STB}}$ — 14 $\overline{\text{AUTOFD}}$ 2 PD0 — 15 $\overline{\text{ERROR}}$ 3 PD1 — 16 $\overline{\text{INIT}}$ 4 PD2 — 17 $\overline{\text{SLCTIN}}$ 5 PD3 — 18 0V 6 PD4 — 19 0V 7 PD5 — 20 0V 8 PD6 — 21 0V 9 PD7 — 22 0V 10 $\overline{\text{ACK}}$ — 23 0V 11 BSY — 24 0V 12 PE — 25 0V 13 SLCT
SK11	Yes	Internal keyboard switch matrix.
SK12	Yes	Internal keyboard switch matrix.
SK15	Yes	6-way mini-DIN socket providing an external connection point for an external keyboard.

Main PCB Links

Link	Fitted	Effect
LK1	Yes	Used to select '5th column' ROM size (JEDEC only device). Size (bits) LK15 up to 1M 2-3 28 pin 2M - 8M 1-2 32 pin
LK2	Yes	Test connector used in conjunction with Acorn designed test equipment: Pin Signal P1 5V P2 D0 P3 LA21 P4 TESTAK P5 RST P6 0V P7 TBA P8 TBA

Switches

Skt	Fitted	Effect
SW1	Yes	Reset
SW2	Yes	RAM size
SW3	Yes	Mem size SW1 SW2 1MB 1-4 1-3 2MB 1-2 1-3 4MB 1-3 1-2

Part 2 – Parts lists

A4 2M final assembly parts list, issue 2

ITEM	PART No.	DESCRIPTION	QTY	Remarks
	0090,260/A	Final Assy Drg		1 Per Batch
	0190,009	Perth Display Unit Assy	1	
	0190,011	Perth UK Keyboard Assy	1	
	0490,043	Perth Base Label	1	
	0290,063	Floppy Disc Flexy Cable	1	Not fitted on this Assy
	0190,074	ON/OFF/Battery Cable Assy	1	
	0290,075	Rear Wall RFI Shield	1	
	0290,076	Main PCB Insulation Sheet	1	
	0290,077	Clamp Plate	1	
	0190,083	DC/DC Convertor PCB Assy	1	Not fitted on this Assy
	0190,085	K/B Rear Edge Carrier	1	
	0190,094	DC Inlet Cable Assembly	1	
	0190,095	Battery LCD Cable Assy	1	
	0290,097	Battery LCD Perspex Windw	1	
	0290,100	Nut M3 Collared captive	3	
	0190,103	Rear Wall RFI Strip	1	
	0290,104	Keyboard Support Collar	3	
	0190,109	Scw M3x4 Pan Head Posi Sp	3	Use on Item 48
	0190,110	Scw 3x8 TC Pan Head PosiS	5	Use on Items 17,48
	0190,112	Scw 3x35 TC Pan Posi Spec	3	Use on Items 6 41
	0290,114	K/B Rear Edge RFI Strip	1	
	0190,115	Floppy Disc Drive Bezel	1	
	0290,117	Battery Status LCD	1	
	0290,118	Floppy D/D RFI Plate	1	
	0290,119	Battery LCD Insulator	1	
	0190,120	Side Drop Flap	1	
	0190,121	Case Lower Sliding Insert	1	
	0190,122	Case Lower (TA/Acorn)	1	
	0190,125	Rear Drop Flap (TA/Acorn)	1	
	0290,135	Foam Strip (Long) 15mm		Not fitted on this Assy
	0190,142	Scw with Washer M3x5	4	Use on Item 73
	0190,145	Rear Wall	1	
	0190,200	Perth (2M) Main PCB Assy	1	
	0800,999	Conrd 4-40UNC Scwlk Stpd	8	
	0800,997	Wshr 4-40UNC Int-Sprl SnP	2	Use on Item 22
	0800,998	Nut 4-40UNC Z&P	2	Use on Item 22
	0805,909	SW SPST DC 2A Roc Snp	1	Use on Item 14
	0895,082	Adh Pad Insulator	4	Use on Item 16
	0907,008	Tape Plstc Blk Insu SFAD 20mm		Use on Items 26,48
	0912,018	Floppy Drive 2MB 3.518mm	1	Not fitted on this Assy
	0940,004	Adh Scw-Lock 222 A/R	Use on Items 56,58	

A4 2M main PCB assy parts list, issue 1

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0290,000	BARE PCB		1
2	0190,200/A	(2M) PCB ASSEMBLY DWG		1 PER BATCH
3	0190,000/C	PCB CIRCUIT DIAGRAM		1 PER BATCH
6	0490,201	PERTH (2M) PCB LABEL	1	
12	0800,071	CONR 2W SHUNT 2mm	1	LK1
13	0870,420	WIRE 22SWG CPR TIN	A/R	X2
15	0902,004	LABEL SERIAL PCB 40x10mm	1	
17	0800,102	SKT IC 42/0.6 SUPA	1	IC4
18	0800,102	SKT IC 42/0.6 SUPA	1	IC15
19	0800,199	SKT STRIP 14/0.1 LP SIL	2	IC18
20	0800,199	SKT STRIP 14/0.1 LP SIL	2	IC19
21	0800,199	SKT STRIP 14/0.1 LP SIL	2	IC21
22	0800,197	SKT STRIP 3/0.1 TURN	1	IC22
23	0800,199	SKT STRIP 14/0.1 LP SIL	2	IC27
24	0800,198	SKT IC 32/0.6 TURN O/F	1	IC38
B1	0817,015	BAT NICAD 1V2 11MAH PCB	1	
C1	0692,333	CPCTR 33N CML 20% 805	1	
C2	0690,220	CPCTR 22P CML 2% 805	1	
C3	0691,102	CPCTR 1N CML 10% 805	1	
C4	0691,102	CPCTR 1N CML 10% 805	1	
C5	0692,333	CPCTR 33N CML 20% 805	1	
C6	0692,104	CPCTR 100N CML 20% 805	1	
C7	0692,103	CPCTR 10N CML 20% 805	1	
C8	0692,473	CPCTR 47N CML 20% 805	1	
C9	0690,220	CPCTR 22P CML 2% 805	1	
C10	0691,102	CPCTR 1N CML 10% 805	1	
C11	0692,333	CPCTR 33N CML 20% 805	1	
C12	0692,473	CPCTR 47N CML 20% 805	1	
C13	0647,002	CPCTR 47U ALEC 16V SMD	1	
C14	0691,102	CPCTR 1N CML 10% 805	1	
C15	0690,220	CPCTR 22P CML 2% 805	1	
C16	0690,150	CPCTR 15P CML 2% 805	1	
C17	0692,333	CPCTR 33N CML 20% 805	1	
C18	0692,333	CPCTR 33N CML 20% 805	1	
C19	0647,001	CPCTR 10U ALEC 16V SMD	1	
C20	0692,333	CPCTR 33N CML 20% 805	1	
C21	0692,333	CPCTR 33N CML 20% 805	1	
C22	0692,333	CPCTR 33N CML 20% 805	1	
C23	0692,473	CPCTR 47N CML 20% 805	1	
C24	0690,220	CPCTR 22P CML 2% 805	1	
C25	0692,104	CPCTR 100N CML 20% 805	1	
C26	0692,473	CPCTR 47N CML 20% 805	1	
C27	0692,104	CPCTR 100N CML 20% 805	1	
C28	0692,473	CPCTR 47N CML 20% 805	1	
C29	0692,473	CPCTR 47N CML 20% 805	1	
C30	0692,473	CPCTR 47N CML 20% 805	1	
C31	0692,473	CPCTR 47N CML 20% 805	1	
C32	0692,473	CPCTR 47N CML 20% 805	1	
C33	0692,473	CPCTR 47N CML 20% 805	1	
C34	0692,104	CPCTR 100N CML 20% 805	1	
C35	0692,333	CPCTR 33N CML 20% 805	1	
C36	0692,333	CPCTR 33N CML 20% 805	1	
C37	0692,333	CPCTR 33N CML 20% 805	1	
C38	0647,002	CPCTR 47U ALEC 16V SMD	1	
C39	0692,473	CPCTR 47N CML 20% 805	1	
C40	0692,333	CPCTR 33N CML 20% 805	1	
C41	0692,333	CPCTR 33N CML 20% 805	1	
C42	0692,333	CPCTR 33N CML 20% 805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
C43	0692,333	CPCTR 33N CML 20% 805	1	
C44	0692,333	CPCTR 33N CML 20% 805	1	
C45	0692,333	CPCTR 33N CML 20% 805	1	
C46	0692,333	CPCTR 33N CML 20% 805	1	
C47	0692,333	CPCTR 33N CML 20% 805	1	
C48	0692,104	CPCTR 100N CML 20% 805	1	
C49	0692,104	CPCTR 100N CML 20% 805	1	
C50	0692,333	CPCTR 33N CML 20% 805	1	
C51	0692,333	CPCTR 33N CML 20% 805	1	
C52	0692,333	CPCTR 33N CML 20% 805	1	
C53	0692,333	CPCTR 33N CML 20% 805	1	
C54	0692,333	CPCTR 33N CML 20% 805	1	
C55	0647,002	CPCTR 47U ALEC 16V SMD	1	
C56	0692,104	CPCTR 100N CML 20% 805	1	
C57	0647,002	CPCTR 47U ALEC 16V SMD	1	
C58	0692,104	CPCTR 100N CML 20% 805	1	
C59	0692,333	CPCTR 33N CML 20% 805	1	
C60	0692,104	CPCTR 100N CML 20% 805	1	
C61	0647,003	CPCTR 100U ALEC 6V3 SMD	1	
C62	0647,002	CPCTR 47U ALEC 16V SMD	1	
C63	0691,102	CPCTR 1N CML 10% 805	1	
C64	0692,333	CPCTR 33N CML 20% 805	1	
C65	0647,001	CPCTR 10U ALEC 16V SMD	1	
C66	0647,002	CPCTR 47U ALEC 16V SMD	1	
C67	0647,001	CPCTR 10U ALEC 16V SMD	1	
C68	0692,333	CPCTR 33N CML 20% 805	1	
C69	0691,102	CPCTR 1N CML 10% 805	1	
C70	0691,102	CPCTR 1N CML 10% 805	1	
C71	0692,104	CPCTR 100N CML 20% 805	1	
C72	0692,104	CPCTR 100N CML 20% 805	1	
C73	0692,104	CPCTR 100N CML 20% 805	1	
C74	0694,272	CPCTR 2N7 CML 5% 805	1	
C75	0681,050	CPCTR 150N CML 5% 1210	1	
C76	0692,333	CPCTR 33N CML 20% 805	1	
C77	0692,473	CPCTR 47N CML 20% 805	1	
C78	0647,002	CPCTR 47U ALEC 16V SMD	1	
C79	0691,102	CPCTR 1N CML 10% 805	1	
C80	0691,102	CPCTR 1N CML 10% 805	1	
C81	0691,102	CPCTR 1N CML 10% 805	1	
C82	0692,104	CPCTR 100N CML 20% 805	1	
C83	0694,223	CPCTR 22N CML 5% 805	1	
C84	0692,104	CPCTR 100N CML 20% 805	1	
C85	0692,473	CPCTR 47N CML 20% 805	1	
C86	0691,102	CPCTR 1N CML 10% 805	1	
C87	0692,333	CPCTR 33N CML 20% 805	1	
C88	0692,473	CPCTR 47N CML 20% 805	1	
C89	0647,002	CPCTR 47U ALEC 16V SMD	1	
C90	0691,102	CPCTR 1N CML 10% 805	1	
C91	0691,102	CPCTR 1N CML 10% 805	1	
C92	0692,473	CPCTR 47N CML 20% 805	1	
C93	0647,001	CPCTR 10U ALEC 16V SMD	1	
C94	0690,220	CPCTR 22P CML 2% 805	1	
C95	0692,473	CPCTR 47N CML 20% 805	1	
C96	0692,104	CPCTR 100N CML 20% 805	1	
C97	0647,003	CPCTR 100U ALEC 6V3 SMD	1	
C98	0692,333	CPCTR 33N CML 20% 805	1	
C99	0692,333	CPCTR 33N CML 20% 805	1	
C100	0691,102	CPCTR 1N CML 10% 805	1	
C101	0691,102	CPCTR 1N CML 10% 805	1	
C102	0647,004	CPCTR 220U ALEC 4V SMD	1	
C103	0692,104	CPCTR 100N CML 20% 805	1	
C104	0691,102	CPCTR 1N CML 10% 805	1	
C105	0692,333	CPCTR 33N CML 20% 805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
C106	0692,333	CPCTR 33N CML 20% 805	1	
C107	0647,000	CPCTR 4U7 ALEC 25V SMD	1	
C108	0647,001	CPCTR 10U ALEC 16V SMD	1	
C109	0691,102	CPCTR 1N CML 10% 805	1	
C110	0691,102	CPCTR 1N CML 10% 805	1	
C111	0691,102	CPCTR 1N CML 10% 805	1	
C112	0691,102	CPCTR 1N CML 10% 805	1	
C113	0692,333	CPCTR 33N CML 20% 805	1	
C114	0691,102	CPCTR 1N CML 10% 805	1	
C115	0692,104	CPCTR 100N CML 20% 805	1	
C116	0690,220	CPCTR 22P CML 2% 805	1	
C117	0690,220	CPCTR 22P CML 2% 805	1	
C118	0691,102	CPCTR 1N CML 10% 805	1	
C119	0691,102	CPCTR 1N CML 10% 805	1	
C120	0691,102	CPCTR 1N CML 10% 805	1	
C121	0691,102	CPCTR 1N CML 10% 805	1	
C122	0691,102	CPCTR 1N CML 10% 805	1	
C123	0692,333	CPCTR 33N CML 20% 805	1	
C124	0692,333	CPCTR 33N CML 20% 805	1	
C125	0681,102	CPCTR 1U TANT SMD 16V 10%	1	
C126	0691,102	CPCTR 1N CML 10% 805	1	
C127	0691,102	CPCTR 1N CML 10% 805	1	
C128	0692,104	CPCTR 100N CML 20% 805	1	
C129	0691,102	CPCTR 1N CML 10% 805	1	
C131	0690,220	CPCTR 22P CML 2% 805	1	
C132	0692,333	CPCTR 33N CML 20% 805	1	
C133	0647,001	CPCTR 10U ALEC 16V SMD	1	
C134	0647,000	CPCTR 4U7 ALEC 25V SMD	1	
C135	0647,001	CPCTR 10U ALEC 16V SMD	1	
C136	0647,000	CPCTR 4U7 ALEC 25V SMD	1	
C137	0647,001	CPCTR 10U ALEC 16V SMD	1	
C138	0647,002	CPCTR 47U ALEC 16V SMD	1	
C139	0692,333	CPCTR 33N CML 20% 805	1	
C140	0692,333	CPCTR 33N CML 20% 805	1	
C141	0692,333	CPCTR 33N CML 20% 805	1	
C142	0692,333	CPCTR 33N CML 20% 805	1	
C143	0692,333	CPCTR 33N CML 20% 805	1	
C500	0692,333	CPCTR 33N CML 20% 805	1	
C501	0692,333	CPCTR 33N CML 20% 805	1	
C502	0692,333	CPCTR 33N CML 20% 805	1	
C503	0692,333	CPCTR 33N CML 20% 805	1	
C504	0692,333	CPCTR 33N CML 20% 805	1	
C505	0692,333	CPCTR 33N CML 20% 805	1	
C506	0692,333	CPCTR 33N CML 20% 805	1	
D1	0796,000	DIODE SI BAS16 SOT23	1	
D2	0796,000	DIODE SI BAS16 SOT23	1	
D3	0796,000	DIODE SI BAS16 SOT23	1	
D5	0796,200	DIODE SI SB 1A/30V SOT89	1	
D6	0796,200	DIODE SI SB 1A/30V SOT89	1	
D7	0796,000	DIODE SI BAS16 SOT23	1	
D8	0796,000	DIODE SI BAS16 SOT23	1	
D9	0796,000	DIODE SI BAS16 SOT23	1	
D10	0796,200	DIODE SI SB 1A/30V SOT89	1	
D11	0796,002	DIODE SI SB 0A1/20V SOT23	1	
D12	0796,002	DIODE SI SB 0A1/20V SOT23	1	
D13	0796,002	DIODE SI SB 0A1/20V SOT23	1	
D16	0796,000	DIODE SI BAS16 SOT23	1	
FS1	0815,500	FUSE 800MA F 63VAC SMD	1	
FS2	0815,501	FUSE 2A F 63VAC SMD	1	
FS3	0815,502	FUSE 4A F 63VAC SMD	1	
IC1	0771,324	IC LM324 QUAD OP AMP SOIC	1	
IC2	0290,031	KBD CTRLR CMOS [708,053]	1	
IC3	0758,086	IC 74AC86 CMOS 14P SOIC	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
IC4	0296,061	RISC OS GREEN (X16) ROM1	1	
IC5	0761,004	IC 74HC04 CMOS 14P SOIC	1	
IC6	0708,584	IC 8583 RTC RAM 8P SOIC	1	
IC7	0292,030	IC IOEB ASIC 100QFP	1	
IC8	0704,125	IC DRAM 64KX4 18PLCC 80NS	1	
IC9	0761,075	IC 74HC75 CMOS 16P SOIC	1	
IC10	0735,241	IC MAX241 RS232 28P SOIC	1	
IC11	0704,125	IC DRAM 64KX4 18PLCC 80NS	1	
IC12	0290,030	IC LC ASIC 100QFP	1	
IC13	2201,368	IC IOC PLSTC	1	
IC14	0771,555	IC 555 TIMER CMOS 8P SOIC	1	
IC15	0296,062	RISC OS GREEN (X16) ROM2	1	
IC16	0758,139	IC 74AC139 CMOS 16P SOIC	1	
IC17	0761,573	IC 74HC573 CMOS 20P SOIC	1	
IC18				NOT FITTED
IC19				NOT FITTED
IC20	0761,573	IC 74HC573 CMOS 20P SOIC	1	
IC21				NOT FITTED
IC22	0702,401	IC DS2400 ID 3W SIL 0.1	1	
IC23	2201,330	ARM3 CPU [PQFP]	1	
IC24	0771,386	IC LM386 AUDIO AMP 8PSOIC	1	
IC25	0771,386	IC LM386 AUDIO AMP 8PSOIC	1	
IC26	0761,365	IC 74HC365 CMOS 16P SOIC	1	
IC27				NOT FITTED
IC28	0761,365	IC 74HC365 CMOS 16P SOIC	1	
IC29	0704,128	IC DRAM 256KX16 80NS SOJ	1	
IC30	0704,129	IC DRAM 256KX16 80NS ZIP	1	
IC32	0771,386	IC LM386 AUDIO AMP 8PSOIC	1	
IC33	0290,032	BATT MGR CTRLR (708,304)	1	
IC34	0701,711	IC 82C711 UCNTRLR 100QFP	1	
IC35	0757,951	IC 74HCT4051 CMOS 16SOIC	1	
IC36	0757,951	IC 74HCT4051 CMOS 16SOIC	1	
IC37	0704,128	IC DRAM 256KX16 80NS SOJ	1	
IC38	0296,063	RISC OS GREEN (PORT) ROM	1	
IC39	0704,129	IC DRAM 256KX16 80NS ZIP	1	
IC40	0758,004	IC 74AC04 CMOS 14P SOIC	1	
IC41	2201,367	IC VIDC 1A PLSTC	1	
IC42	0762,573	IC 74HCT573 CMOS 20P SOIC	1	
IC43	0761,573	IC 74HC573 CMOS 20P SOIC	1	
IC44	0700,104	IC MEMC1A 12MHZ PLSTC	1	
IC45	0762,573	IC 74HCT573 CMOS 20P SOIC	1	
IC46	0761,573	IC 74HC573 CMOS 20P SOIC	1	
L1	0860,500	CHOKE 80R/100MHZ SMD	1	
L3	0860,500	CHOKE 80R/100MHZ SMD	1	
L4	0860,500	CHOKE 80R/100MHZ SMD	1	
L8	0860,500	CHOKE 80R/100MHZ SMD	1	
L10	0860,500	CHOKE 80R/100MHZ SMD	1	
L11	0860,500	CHOKE 80R/100MHZ SMD	1	
L15	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L16	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L17	0860,501	IND EMI FLTER 100PF SMD	1	
L18	0860,501	IND EMI FLTER 100PF SMD	1	
L19	0860,501	IND EMI FLTER 100PF SMD	1	
L20	0860,501	IND EMI FLTER 100PF SMD	1	
L21	0860,502	IND EMI FILTER 2N2 SMD	1	
L24	0860,502	IND EMI FILTER 2N2 SMD	1	
L25	0860,501	IND EMI FLTER 100PF SMD	1	
L26	0860,501	IND EMI FLTER 100PF SMD	1	
L27	0860,502	IND EMI FILTER 2N2 SMD	1	
L28	0860,502	IND EMI FILTER 2N2 SMD	1	
L29	0860,501	IND EMI FLTER 100PF SMD	1	
L30	0860,502	IND EMI FILTER 2N2 SMD	1	
L31	0860,501	IND EMI FLTER 100PF SMD	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
L32	0860,502	IND EMI FILTER 2N2 SMD	1	
L33	0860,502	IND EMI FILTER 2N2 SMD	1	
L34	0860,502	IND EMI FILTER 2N2 SMD	1	
L35	0860,502	IND EMI FILTER 2N2 SMD	1	
L36	0860,502	IND EMI FILTER 2N2 SMD	1	
L37	0860,501	IND EMI FLTER 100PF SMD	1	
L38	0860,502	IND EMI FILTER 2N2 SMD	1	
L39	0860,502	IND EMI FILTER 2N2 SMD	1	
L40	0860,501	IND EMI FLTER 100PF SMD	1	
L41	0860,502	IND EMI FILTER 2N2 SMD	1	
L42	0860,502	IND EMI FILTER 2N2 SMD	1	
L43	0860,502	IND EMI FILTER 2N2 SMD	1	
LK1	0804,007	CONR 3W WAFR SIL 2MM STR	1	
LK2	0804,009	CONR 9W WAFR SIL 2MM STR	1	
LK55				NOT FITTED
PL1	0800,297	CONRD 9WPLG RA PCB+RFI+L	1	
PL2	0804,004	CONR 16W STAKE 2ROW 2mmP	2	
PL3	0804,011	CONR 26W BOX HDR 2ROW 2MM	1	
PL4	0804,010	CONR 6W HDR SIL 2MM LK	1	
PL5	0804,000	CONR 6W BOX HDR 2ROW 2MM	1	
PL6	0804,001	CONR 10W BOX HDR 2ROW 2MM	1	
PL7	0804,005	CONR 10W WAFR 2ROW 2MM ST	1	
Q1	0778,212	VOLT REG 78L12 12V 8PSOIC	1	
Q2	0778,205	VOLT REG 5V UPWR TO92	1	
Q3	0784,849	TRANS BC849C NPN SOT23	1	
Q4	0784,859	TRANS BC859C PNP SOT23	1	
Q5	0784,859	TRANS BC859C PNP SOT23	1	
Q6	0784,849	TRANS BC849C NPN SOT23	1	
Q7	0784,849	TRANS BC849C NPN SOT23	1	
R1	0523,333	RES 33K SMD 5% 0W10 0805	1	
R2	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R3	0523,471	RES 470R SMD 5% 0W10 0805	1	
R4	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R5	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R6	0523,183	RES 18K SMD 5% 0W10 0805	1	
R7	0523,104	RES 100K SMD 5% 0W10 0805	1	
R8	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R9	0523,680	RES 68R SMD 5% 0W10 0805	1	
R10	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R11	0523,331	RES 330R SMD 5% 0W10 0805	1	
R12	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R13	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R14	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R15	0523,680	RES 68R SMD 5% 0W10 0805	1	
R16	0523,103	RES 10K SMD 5% 0W10 0805	1	
R17	0523,223	RES 22K SMD 5% 0W10 0805	1	
R18	0523,183	RES 18K SMD 5% 0W10 0805	1	
R19	0523,223	RES 22K SMD 5% 0W10 0805	1	
R20	0523,680	RES 68R SMD 5% 0W10 0805	1	
R21	0523,221	RES 220R SMD 5% 0W10 0805	1	
R22	0523,330	RES 33R SMD 5% 0W10 0805	1	
R23	0523,330	RES 33R SMD 5% 0W10 0805	1	
R24	0523,680	RES 68R SMD 5% 0W10 0805	1	
R25	0523,223	RES 22K SMD 5% 0W10 0805	1	
R26	0523,330	RES 33R SMD 5% 0W10 0805	1	
R27	0523,105	RES 1M0 SMD 5% 0W10 0805	1	
R28	0523,330	RES 33R SMD 5% 0W10 0805	1	
R29	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R30	0523,330	RES 33R SMD 5% 0W10 0805	1	
R31	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R32	0523,330	RES 33R SMD 5% 0W10 0805	1	
R33	0523,331	RES 330R SMD 5% 0W10 0805	1	
R34	0523,152	RES 1K5 SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R35	0523,331	RES 330R SMD 5% 0W10 0805	1	
R36	0523,331	RES 330R SMD 5% 0W10 0805	1	
R37	0523,104	RES 100K SMD 5% 0W10 0805	1	
R38	0523,104	RES 100K SMD 5% 0W10 0805	1	
R39	0523,104	RES 100K SMD 5% 0W10 0805	1	
R40	0523,103	RES 10K SMD 5% 0W10 0805	1	
R41	0523,104	RES 100K SMD 5% 0W10 0805	1	
R42	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R43	0523,330	RES 33R SMD 5% 0W10 0805	1	
R44	0523,330	RES 33R SMD 5% 0W10 0805	1	
R45	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R46	0523,561	RES 560R SMD 5% 0W10 0805	1	
R47	0523,100	RES 10R SMD 5% 0W10 0805	1	
R48	0523,330	RES 33R SMD 5% 0W10 0805	1	
R49	0523,680	RES 68R SMD 5% 0W10 0805	1	
R50	0523,680	RES 68R SMD 5% 0W10 0805	1	
R51	0523,680	RES 68R SMD 5% 0W10 0805	1	
R52	0523,680	RES 68R SMD 5% 0W10 0805	1	
R53	0523,680	RES 68R SMD 5% 0W10 0805	1	
R54	0523,680	RES 68R SMD 5% 0W10 0805	1	
R55	0523,680	RES 68R SMD 5% 0W10 0805	1	
R56	0523,680	RES 68R SMD 5% 0W10 0805	1	
R57	0523,680	RES 68R SMD 5% 0W10 0805	1	
R58	0523,680	RES 68R SMD 5% 0W10 0805	1	
R59	0523,680	RES 68R SMD 5% 0W10 0805	1	
R60	0523,680	RES 68R SMD 5% 0W10 0805	1	
R61	0523,680	RES 68R SMD 5% 0W10 0805	1	
R62	0523,680	RES 68R SMD 5% 0W10 0805	1	
R63	0523,680	RES 68R SMD 5% 0W10 0805	1	
R64	0523,680	RES 68R SMD 5% 0W10 0805	1	
R65	0523,680	RES 68R SMD 5% 0W10 0805	1	
R66	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R67	0523,330	RES 33R SMD 5% 0W10 0805	1	
R68	0523,473	RES 47K SMD 5% 0W10 0805	1	
R69	0523,473	RES 47K SMD 5% 0W10 0805	1	
R70	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R71	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R72	0523,330	RES 33R SMD 5% 0W10 0805	1	
R73	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R74	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R75	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R76	0523,473	RES 47K SMD 5% 0W10 0805	1	
R77	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R78	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R79	0523,330	RES 33R SMD 5% 0W10 0805	1	
R80	0523,183	RES 18K SMD 5% 0W10 0805	1	
R81	0523,330	RES 33R SMD 5% 0W10 0805	1	
R82	0523,100	RES 10R SMD 5% 0W10 0805	1	
R83	0523,330	RES 33R SMD 5% 0W10 0805	1	
R84	0523,221	RES 220R SMD 5% 0W10 0805	1	
R85	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R86	0523,331	RES 330R SMD 5% 0W10 0805	1	
R87	0523,680	RES 68R SMD 5% 0W10 0805	1	
R88	0523,561	RES 560R SMD 5% 0W10 0805	1	
R89	0523,103	RES 10K SMD 5% 0W10 0805	1	
R90	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R91	0523,330	RES 33R SMD 5% 0W10 0805	1	
R92	0523,183	RES 18K SMD 5% 0W10 0805	1	
R93	0523,223	RES 22K SMD 5% 0W10 0805	1	
R94	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R95	0523,105	RES 1M0 SMD 5% 0W10 0805	1	
R96	0523,330	RES 33R SMD 5% 0W10 0805	1	
R97	0523,183	RES 18K SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R98	0523,330	RES 33R SMD 5% 0W10 0805	1	
R99	0523,223	RES 22K SMD 5% 0W10 0805	1	
R100	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R101	0523,330	RES 33R SMD 5% 0W10 0805	1	
R102	0509,001	RES 0R33 0W5 1% AXIAL	1	
R103	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R104	0509,001	RES 0R33 0W5 1% AXIAL	1	
R105	0523,331	RES 330R SMD 5% 0W10 0805	1	
R106	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R107	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R108	0523,100	RES 10R SMD 5% 0W10 0805	1	
R109	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R110	0523,331	RES 330R SMD 5% 0W10 0805	1	
R111	0523,103	RES 10K SMD 5% 0W10 0805	1	
R112	0523,330	RES 33R SMD 5% 0W10 0805	1	
R113	0523,103	RES 10K SMD 5% 0W10 0805	1	
R114	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R115	0523,680	RES 68R SMD 5% 0W10 0805	1	
R116	0523,680	RES 68R SMD 5% 0W10 0805	1	
R117	0523,680	RES 68R SMD 5% 0W10 0805	1	
R118	0523,680	RES 68R SMD 5% 0W10 0805	1	
R119	0523,680	RES 68R SMD 5% 0W10 0805	1	
R120	0523,680	RES 68R SMD 5% 0W10 0805	1	
R121	0523,680	RES 68R SMD 5% 0W10 0805	1	
R122	0523,680	RES 68R SMD 5% 0W10 0805	1	
R123	0523,680	RES 68R SMD 5% 0W10 0805	1	
R124	0523,680	RES 68R SMD 5% 0W10 0805	1	
R125	0523,680	RES 68R SMD 5% 0W10 0805	1	
R126	0523,680	RES 68R SMD 5% 0W10 0805	1	
R127	0523,680	RES 68R SMD 5% 0W10 0805	1	
R128	0523,680	RES 68R SMD 5% 0W10 0805	1	
R129	0523,220	RES 22R SMD 5% 0W10 0805	1	
R130	0523,220	RES 22R SMD 5% 0W10 0805	1	
R131	0523,220	RES 22R SMD 5% 0W10 0805	1	
R132	0523,220	RES 22R SMD 5% 0W10 0805	1	
R133	0523,220	RES 22R SMD 5% 0W10 0805	1	
R134	0523,331	RES 330R SMD 5% 0W10 0805	1	
R135	0523,103	RES 10K SMD 5% 0W10 0805	1	
R136	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R137	0523,680	RES 68R SMD 5% 0W10 0805	1	
R138	0523,331	RES 330R SMD 5% 0W10 0805	1	
R139	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R140	0523,330	RES 33R SMD 5% 0W10 0805	1	
R141	0523,330	RES 33R SMD 5% 0W10 0805	1	
R142	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R143	0523,103	RES 10K SMD 5% 0W10 0805	1	
R144	0523,331	RES 330R SMD 5% 0W10 0805	1	
R145	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R146	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R147	0523,332	RES 3K3 SMD 5% 0W10 0805	1	
R148	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R149	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R150	0523,330	RES 33R SMD 5% 0W10 0805	1	
R151	0523,330	RES 33R SMD 5% 0W10 0805	1	
R152	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R153	0523,330	RES 33R SMD 5% 0W10 0805	1	
R154	0523,330	RES 33R SMD 5% 0W10 0805	1	
R155	0523,103	RES 10K SMD 5% 0W10 0805	1	
R156	0523,330	RES 33R SMD 5% 0W10 0805	1	
R157	0523,330	RES 33R SMD 5% 0W10 0805	1	
R158	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R159	0523,330	RES 33R SMD 5% 0W10 0805	1	
R160	0523,472	RES 4K7 SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R161	0523,330	RES 33R SMD 5% 0W10 0805	1	
R162	0523,330	RES 33R SMD 5% 0W10 0805	1	
R163	0523,330	RES 33R SMD 5% 0W10 0805	1	
R164	0523,103	RES 10K SMD 5% 0W10 0805	1	
R165	0523,330	RES 33R SMD 5% 0W10 0805	1	
R166	0523,330	RES 33R SMD 5% 0W10 0805	1	
R167	0523,330	RES 33R SMD 5% 0W10 0805	1	
R168	0523,330	RES 33R SMD 5% 0W10 0805	1	
R169	0523,330	RES 33R SMD 5% 0W10 0805	1	
R170	0523,331	RES 330R SMD 5% 0W10 0805	1	
R171	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R172	0523,222	RES 2K2 SMD 5% 0W10 0805	1	
R173	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R174	0523,104	RES 100K SMD 5% 0W10 0805	1	
R175	0523,271	RES 270R SMD 5% 0W10 0805	1	
R176	0523,301	RES 300R SMD 5% 0W10 0805	1	
R177	0523,135	RES 1M3 SMD 5% 0W10 0805	1	
R178	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R179	0523,101	RES 100R SMD 5% 0W10 0805	1	
R180	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R181	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R182	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R183	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R184	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R185	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R186	0523,222	RES 2K2 SMD 5% 0W10 0805	1	
R187	0523,222	RES 2K2 SMD 5% 0W10 0805	1	
R188	0523,221	RES 220R SMD 5% 0W10 0805	1	
R189	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R190	0523,223	RES 22K SMD 5% 0W10 0805	1	
R191	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R192	0523,101	RES 100R SMD 5% 0W10 0805	1	
R193	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R194	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R195	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R196	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R197	0523,105	RES 1M0 SMD 5% 0W10 0805	1	
R198	0523,332	RES 3K3 SMD 5% 0W10 0805	1	
R199	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R200	0522,425	RES 18K2 SMD 1% 0W25 1206	1	
R201	0523,332	RES 3K3 SMD 5% 0W10 0805	1	
R202	0523,103	RES 10K SMD 5% 0W10 0805	1	
R203	0522,317	RES 1K50 SMD 1% 0W25 1206	1	
R204	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R205	0522,380	RES 6K81 SMD 1% 0W25 1206	1	
R206	0522,450	RES 33K2 SMD 1% 0W25 1206	1	
R207	0523,101	RES 100R SMD 5% 0W10 0805	1	
R208	0523,271	RES 270R SMD 5% 0W10 0805	1	
R209	0522,500	RES 100K SMD 1% 0W25 1206	1	
R210	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R211	0523,271	RES 270R SMD 5% 0W10 0805	1	
R212	0522,558	RES 402K SMD 1% 0W25 1206	1	
R213	0523,680	RES 68R SMD 5% 0W10 0805	1	
R214	0523,104	RES 100K SMD 5% 0W10 0805	1	
R215	0525,202	RES 2K0 SMD .1% 0W1 1206	1	
R216	0525,152	RES 1K5 SMD .1% 0W1 1206	1	
R217	0525,163	RES 16K SMD .1% 0W1 1206	1	
R218	0523,823	RES 82K SMD 5% 0W10 0805	1	
R219	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R220	0523,103	RES 10K SMD 5% 0W10 0805	1	
R221	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R222	0523,183	RES 18K SMD 5% 0W10 0805	1	
R223	0523,471	RES 470R SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R224	0523,103	RES 10K SMD 5% 0W10 0805	1	
R225	0523,103	RES 10K SMD 5% 0W10 0805	1	
R226	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R227	0523,680	RES 68R SMD 5% 0W10 0805	1	
R228	0523,680	RES 68R SMD 5% 0W10 0805	1	
R229	0523,680	RES 68R SMD 5% 0W10 0805	1	
R230	0523,680	RES 68R SMD 5% 0W10 0805	1	
R231	0523,680	RES 68R SMD 5% 0W10 0805	1	
R232	0523,103	RES 10K SMD 5% 0W10 0805	1	
R503	0523,680	RES 68R SMD 5% 0W10 0805	1	
R504	0523,680	RES 68R SMD 5% 0W10 0805	1	
R505	0523,680	RES 68R SMD 5% 0W10 0805	1	
R506	0523,680	RES 68R SMD 5% 0W10 0805	1	
R507	0523,680	RES 68R SMD 5% 0W10 0805	1	
R508	0523,680	RES 68R SMD 5% 0W10 0805	1	
R509	0523,680	RES 68R SMD 5% 0W10 0805	1	
R510	0523,680	RES 68R SMD 5% 0W10 0805	1	
R511	0523,680	RES 68R SMD 5% 0W10 0805	1	
R512	0523,680	RES 68R SMD 5% 0W10 0805	1	
R513	0523,680	RES 68R SMD 5% 0W10 0805	1	
R514	0523,680	RES 68R SMD 5% 0W10 0805	1	
R515	0523,680	RES 68R SMD 5% 0W10 0805	1	
R516	0523,680	RES 68R SMD 5% 0W10 0805	1	
R517	0523,680	RES 68R SMD 5% 0W10 0805	1	
R518	0523,680	RES 68R SMD 5% 0W10 0805	1	
R519	0523,104	RES 100K SMD 5% 0W10 0805	1	
R520	0523,104	RES 100K SMD 5% 0W10 0805	1	
R521	0523,104	RES 100K SMD 5% 0W10 0805	1	
R522	0523,104	RES 100K SMD 5% 0W10 0805	1	
R523	0523,104	RES 100K SMD 5% 0W10 0805	1	
R524	0523,104	RES 100K SMD 5% 0W10 0805	1	
R525	0523,104	RES 100K SMD 5% 0W10 0805	1	
R526	0523,104	RES 100K SMD 5% 0W10 0805	1	
R527	0523,104	RES 100K SMD 5% 0W10 0805	1	
R528	0523,104	RES 100K SMD 5% 0W10 0805	1	
R529	0523,104	RES 100K SMD 5% 0W10 0805	1	
R549	0523,104	RES 100K SMD 5% 0W10 0805	1	
R551	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R552	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
SK1	0800,925	CONR 9W MINDIN RAPCB MRFI	1	
SK2	0800,645	CONR 3,5MM RA PCB JKSKT	1	
SK3	0801,203	CONR 20W FPC 1MMP ST ZIF	1	
SK4	0801,203	CONR 20W FPC 1MMP ST ZIF	1	
SK5	0801,206	CONR 26W 1,25 RA FPC ZIF	1	
SK6	0800,995	CONRD 15WSKT RA HD+RFI+L	1	
SK7	0194,008	VIDEO HYBRID 15P	1	
SK10	0898,005	CONRD 25WSKT RA PCB+RF+L	1	
SK11	0801,204	CONR 8W 1,25MM ST CIC ZIF	1	
SK12	0801,205	CONR 20W 1,25 ST CIC ZIF	1	
SK15	0800,923	CONR 6W MINDIN RAPCB MRFI	1	
SW1	0805,709	SW 1P MOM PTM P/B RA PCB	1	
SW2	0805,125	SW SP 3W CO ROTARY SMD	1	
SW3	0805,126	SW SPCO ROTARY SMD	1	
X1	0820,243	XTAL 24MHZ HC49 5,08MMH	1	
X2	0821,327	XTAL 32.768KHZ CC 0.05P	1	
X3	0820,253	XTAL 25.175MHZ HC49 5,08H	1	
X4	0820,243	XTAL 24MHZ HC49 5,08MMH	1	
X5	0820,363	XTAL OSC 36MHZ CMOS 8P PL	1	
X6	0820,041	XTAL 4.194304M HC49 5,08H	1	
Z1	0796,102	DIODE 3V9 ZNR 0W3 SOT23	1	
Z2	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z3	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z4	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
Z5	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z6	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z7	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z8	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z9	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z10	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z11	0796,103	DIODE 5V1 ZNR 0W3 SOT23	1	
Z12	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	

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ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0290,000	BARE PCB		1
2	0190,260/A	(4M) PCB ASSEMBLY DWG		1 PER BATCH
3	0190,000/C	PCB CIRCUIT DIAGRAM		1 PER BATCH
6	0490,261	PERTH (4M) PCB LABEL	1	
12	0800,071	CONN 2W SHUNT 2mm	1	LK1
13	0870,420	WIRE 22SWG CPR TIN	A/R	X2
15	0902,004	LABEL SERIAL PCB 40x10mm	1	
17	0800,102	SKT IC 42/0.6 SUPA	1	IC4
18	0800,102	SKT IC 42/0.6 SUPA	1	IC15
22	0800,197	SKT STRIP 3/0.1 TURN	1	IC22
24	0800,198	SKT IC 32/0.6 TURN O/F	1	IC38
B1	0817,015	BAT NICAD 1V2 11MAH PCB	1	
C1	0692,333	CPCTR 33N CML 20% 805	1	
C2	0690,220	CPCTR 22P CML 2% 805	1	
C3	0691,102	CPCTR 1N CML 10% 805	1	
C4	0691,102	CPCTR 1N CML 10% 805	1	
C5	0692,333	CPCTR 33N CML 20% 805	1	
C6	0692,104	CPCTR 100N CML 20% 805	1	
C7	0692,103	CPCTR 10N CML 20% 805	1	
C8	0692,473	CPCTR 47N CML 20% 805	1	
C9	0690,220	CPCTR 22P CML 2% 805	1	
C10	0691,102	CPCTR 1N CML 10% 805	1	
C11	0692,333	CPCTR 33N CML 20% 805	1	
C12	0692,473	CPCTR 47N CML 20% 805	1	
C13	0647,002	CPCTR 47U ALEC 16V SMD	1	
C14	0691,102	CPCTR 1N CML 10% 805	1	
C15	0690,220	CPCTR 22P CML 2% 805	1	
C16	0690,150	CPCTR 15P CML 2% 805	1	
C17	0692,333	CPCTR 33N CML 20% 805	1	
C18	0692,333	CPCTR 33N CML 20% 805	1	
C19	0647,001	CPCTR 10U ALEC 16V SMD	1	
C20	0692,333	CPCTR 33N CML 20% 805	1	
C21	0692,333	CPCTR 33N CML 20% 805	1	
C22	0692,333	CPCTR 33N CML 20% 805	1	
C23	0692,473	CPCTR 47N CML 20% 805	1	
C24	0690,220	CPCTR 22P CML 2% 805	1	
C25	0692,104	CPCTR 100N CML 20% 805	1	
C26	0692,473	CPCTR 47N CML 20% 805	1	
C27	0692,104	CPCTR 100N CML 20% 805	1	
C28	0692,473	CPCTR 47N CML 20% 805	1	
C29	0692,473	CPCTR 47N CML 20% 805	1	
C30	0692,473	CPCTR 47N CML 20% 805	1	
C31	0692,473	CPCTR 47N CML 20% 805	1	
C32	0692,473	CPCTR 47N CML 20% 805	1	
C33	0692,473	CPCTR 47N CML 20% 805	1	
C34	0692,104	CPCTR 100N CML 20% 805	1	
C35	0692,333	CPCTR 33N CML 20% 805	1	
C36	0692,333	CPCTR 33N CML 20% 805	1	
C37	0692,333	CPCTR 33N CML 20% 805	1	
C38	0647,002	CPCTR 47U ALEC 16V SMD	1	
C39	0692,473	CPCTR 47N CML 20% 805	1	
C40	0692,333	CPCTR 33N CML 20% 805	1	
C41	0692,333	CPCTR 33N CML 20% 805	1	
C42	0692,333	CPCTR 33N CML 20% 805	1	
C43	0692,333	CPCTR 33N CML 20% 805	1	
C44	0692,333	CPCTR 33N CML 20% 805	1	
C45	0692,333	CPCTR 33N CML 20% 805	1	
C46	0692,333	CPCTR 33N CML 20% 805	1	
C47	0692,333	CPCTR 33N CML 20% 805	1	
C48	0692,104	CPCTR 100N CML 20% 805	1	
C49	0692,104	CPCTR 100N CML 20% 805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
C50	0692,333	CPCTR 33N CML 20% 805	1	
C51	0692,333	CPCTR 33N CML 20% 805	1	
C52	0692,333	CPCTR 33N CML 20% 805	1	
C53	0692,333	CPCTR 33N CML 20% 805	1	
C54	0692,333	CPCTR 33N CML 20% 805	1	
C55	0647,002	CPCTR 47U ALEC 16V SMD	1	
C56	0692,104	CPCTR 100N CML 20% 805	1	
C57	0647,002	CPCTR 47U ALEC 16V SMD	1	
C58	0692,104	CPCTR 100N CML 20% 805	1	
C59	0692,333	CPCTR 33N CML 20% 805	1	
C60	0692,104	CPCTR 100N CML 20% 805	1	
C61	0647,003	CPCTR 100U ALEC 6V3 SMD	1	
C62	0647,002	CPCTR 47U ALEC 16V SMD	1	
C63	0691,102	CPCTR 1N CML 10% 805	1	
C64	0692,333	CPCTR 33N CML 20% 805	1	
C65	0647,001	CPCTR 10U ALEC 16V SMD	1	
C66	0647,002	CPCTR 47U ALEC 16V SMD	1	
C67	0647,001	CPCTR 10U ALEC 16V SMD	1	
C68	0692,333	CPCTR 33N CML 20% 805	1	
C69	0691,102	CPCTR 1N CML 10% 805	1	
C70	0691,102	CPCTR 1N CML 10% 805	1	
C71	0692,104	CPCTR 100N CML 20% 805	1	
C72	0692,104	CPCTR 100N CML 20% 805	1	
C73	0692,104	CPCTR 100N CML 20% 805	1	
C74	0694,272	CPCTR 2N7 CML 5% 805	1	
C75	0681,050	CPCTR 150N CML 5% 1210	1	
C76	0692,333	CPCTR 33N CML 20% 805	1	
C77	0692,473	CPCTR 47N CML 20% 805	1	
C78	0647,002	CPCTR 47U ALEC 16V SMD	1	
C79	0691,102	CPCTR 1N CML 10% 805	1	
C80	0691,102	CPCTR 1N CML 10% 805	1	
C81	0691,102	CPCTR 1N CML 10% 805	1	
C82	0692,104	CPCTR 100N CML 20% 805	1	
C83	0694,223	CPCTR 22N CML 5% 805	1	
C84	0692,104	CPCTR 100N CML 20% 805	1	
C85	0692,473	CPCTR 47N CML 20% 805	1	
C86	0691,102	CPCTR 1N CML 10% 805	1	
C87	0692,333	CPCTR 33N CML 20% 805	1	
C88	0692,473	CPCTR 47N CML 20% 805	1	
C89	0647,002	CPCTR 47U ALEC 16V SMD	1	
C90	0691,102	CPCTR 1N CML 10% 805	1	
C91	0691,102	CPCTR 1N CML 10% 805	1	
C92	0692,473	CPCTR 47N CML 20% 805	1	
C93	0647,001	CPCTR 10U ALEC 16V SMD	1	
C94	0690,220	CPCTR 22P CML 2% 805	1	
C95	0692,473	CPCTR 47N CML 20% 805	1	
C96	0692,104	CPCTR 100N CML 20% 805	1	
C97	0647,003	CPCTR 100U ALEC 6V3 SMD	1	
C98	0692,333	CPCTR 33N CML 20% 805	1	
C99	0692,333	CPCTR 33N CML 20% 805	1	
C100	0691,102	CPCTR 1N CML 10% 805	1	
C101	0691,102	CPCTR 1N CML 10% 805	1	
C102	0647,004	CPCTR 220U ALEC 4V SMD	1	
C103	0692,104	CPCTR 100N CML 20% 805	1	
C104	0691,102	CPCTR 1N CML 10% 805	1	
C105	0692,333	CPCTR 33N CML 20% 805	1	
C106	0692,333	CPCTR 33N CML 20% 805	1	
C107	0647,000	CPCTR 4U7 ALEC 25V SMD	1	
C108	0647,001	CPCTR 10U ALEC 16V SMD	1	
C109	0691,102	CPCTR 1N CML 10% 805	1	
C110	0691,102	CPCTR 1N CML 10% 805	1	
C111	0691,102	CPCTR 1N CML 10% 805	1	
C112	0691,102	CPCTR 1N CML 10% 805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
C113	0692,333	CPCTR 33N CML 20% 805	1	
C114	0691,102	CPCTR 1N CML 10% 805	1	
C115	0692,104	CPCTR 100N CML 20% 805	1	
C116	0690,220	CPCTR 22P CML 2% 805	1	
C117	0690,220	CPCTR 22P CML 2% 805	1	
C118	0691,102	CPCTR 1N CML 10% 805	1	
C119	0691,102	CPCTR 1N CML 10% 805	1	
C120	0691,102	CPCTR 1N CML 10% 805	1	
C121	0691,102	CPCTR 1N CML 10% 805	1	
C122	0691,102	CPCTR 1N CML 10% 805	1	
C123	0692,333	CPCTR 33N CML 20% 805	1	
C124	0692,333	CPCTR 33N CML 20% 805	1	
C125	0681,102	CPCTR 1U TANT SMD 16V 10%	1	
C126	0691,102	CPCTR 1N CML 10% 805	1	
C127	0691,102	CPCTR 1N CML 10% 805	1	
C128	0692,104	CPCTR 100N CML 20% 805	1	
C129	0691,102	CPCTR 1N CML 10% 805	1	
C131	0690,220	CPCTR 22P CML 2% 805	1	
C132	0692,333	CPCTR 33N CML 20% 805	1	
C133	0647,001	CPCTR 10U ALEC 16V SMD	1	
C134	0647,000	CPCTR 4U7 ALEC 25V SMD	1	
C135	0647,001	CPCTR 10U ALEC 16V SMD	1	
C136	0647,000	CPCTR 4U7 ALEC 25V SMD	1	
C137	0647,001	CPCTR 10U ALEC 16V SMD	1	
C138	0647,002	CPCTR 47U ALEC 16V SMD	1	
C139	0692,333	CPCTR 33N CML 20% 805	1	
C140	0692,333	CPCTR 33N CML 20% 805	1	
C141	0692,333	CPCTR 33N CML 20% 805	1	
C142	0692,333	CPCTR 33N CML 20% 805	1	
C143	0692,333	CPCTR 33N CML 20% 805	1	
C500	0692,333	CPCTR 33N CML 20% 805	1	
C501	0692,333	CPCTR 33N CML 20% 805	1	
C502	0692,333	CPCTR 33N CML 20% 805	1	
C503	0692,333	CPCTR 33N CML 20% 805	1	
C504	0692,333	CPCTR 33N CML 20% 805	1	
C505	0692,333	CPCTR 33N CML 20% 805	1	
C506	0692,333	CPCTR 33N CML 20% 805	1	
D1	0796,000	DIODE SI BAS16 SOT23	1	
D2	0796,000	DIODE SI BAS16 SOT23	1	
D3	0796,000	DIODE SI BAS16 SOT23	1	
D5	0796,200	DIODE SI SB 1A/30V SOT89	1	
D6	0796,200	DIODE SI SB 1A/30V SOT89	1	
D7	0796,000	DIODE SI BAS16 SOT23	1	
D8	0796,000	DIODE SI BAS16 SOT23	1	
D9	0796,000	DIODE SI BAS16 SOT23	1	
D10	0796,200	DIODE SI SB 1A/30V SOT89	1	
D11	0796,002	DIODE SI SB 0A1/20V SOT23	1	
D12	0796,002	DIODE SI SB 0A1/20V SOT23	1	
D13	0796,002	DIODE SI SB 0A1/20V SOT23	1	
D16	0796,000	DIODE SI BAS16 SOT23	1	
FS1	0815,500	FUSE 800MA F 63VAC SMD	1	
FS2	0815,501	FUSE 2A F 63VAC SMD	1	
FS3	0815,502	FUSE 4A F 63VAC SMD	1	
IC1	0771,324	IC LM324 QUAD OP AMP SOIC	1	
IC2	0290,031	KBD CTRLR CMOS [708,053]	1	
IC3	0758,086	IC 74AC86 CMOS 14P SOIC	1	
IC4	0296,061	RISC OS GREEN (X16) ROM1	1	
IC5	0761,004	IC 74HC04 CMOS 14P SOIC	1	
IC6	0708,584	IC 8583 RTC RAM 8P SOIC	1	
IC7	0292,030	IC IOEB ASIC 100QFP	1	
IC8	0704,125	IC DRAM 64KX4 18PLCC 80NS	1	
IC9	0761,075	IC 74HC75 CMOS 16P SOIC	1	
IC10	0735,241	IC MAX241 RS232 28P SOIC	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
IC11	0704,125	IC DRAM 64KX4 18PLCC 80NS	1	
IC12	0290,030	IC LC ASIC 100QFP	1	
IC13	2201,368	IC IOC PLSTC	1	
IC14	0771,555	IC 555 TIMER CMOS 8P SOIC	1	
IC15	0296,062	RISC OS GREEN (X16) ROM2	1	
IC16	0758,139	IC 74AC139 CMOS 16P SOIC	1	
IC17	0761,573	IC 74HC573 CMOS 20P SOIC	1	
IC18	0704,127	IC DRAM 512KX8 80NS ZIP	1	
IC19	0704,127	IC DRAM 512KX8 80NS ZIP	1	
IC20	0761,573	IC 74HC573 CMOS 20P SOIC	1	
IC21	0704,127	IC DRAM 512KX8 80NS ZIP	1	
IC22	0702,401	IC DS2400 ID 3W SIL 0.1	1	
IC23	2201,330	ARM3 CPU [PQFP]	1	
IC24	0771,386	IC LM386 AUDIO AMP 8PSOIC	1	
IC25	0771,386	IC LM386 AUDIO AMP 8PSOIC	1	
IC26	0761,365	IC 74HC365 CMOS 16P SOIC	1	
IC27	0704,127	IC DRAM 512KX8 80NS ZIP	1	
IC28	0761,365	IC 74HC365 CMOS 16P SOIC	1	
IC29	0704,128	IC DRAM 256KX16 80NS SOJ	1	
IC30	0704,129	IC DRAM 256KX16 80NS ZIP	1	
IC32	0771,386	IC LM386 AUDIO AMP 8PSOIC	1	
IC33	0290,032	BATT MGR CTRLR (708,304)	1	
IC34	0701,711	IC 82C711 UCNTRLR 100QFP	1	
IC35	0757,951	IC 74HCT4051 CMOS 16SOIC	1	
IC36	0757,951	IC 74HCT4051 CMOS 16SOIC	1	
IC37	0704,128	IC DRAM 256KX16 80NS SOJ	1	
IC38	0296,063	RISC OS GREEN (PORT) ROM	1	
IC39	0704,129	IC DRAM 256KX16 80NS ZIP	1	
IC40	0758,004	IC 74AC04 CMOS 14P SOIC	1	
IC41	2201,367	IC VIDC 1A PLSTC	1	
IC42	0762,573	IC 74HCT573 CMOS 20P SOIC	1	
IC43	0761,573	IC 74HC573 CMOS 20P SOIC	1	
IC44	0700,104	IC MEMC1A 12MHZ PLSTC	1	
IC45	0762,573	IC 74HCT573 CMOS 20P SOIC	1	
IC46	0761,573	IC 74HC573 CMOS 20P SOIC	1	
L1	0860,500	CHOKE 80R/100MHZ SMD	1	
L3	0860,500	CHOKE 80R/100MHZ SMD	1	
L4	0860,500	CHOKE 80R/100MHZ SMD	1	
L8	0860,500	CHOKE 80R/100MHZ SMD	1	
L10	0860,500	CHOKE 80R/100MHZ SMD	1	
L11	0860,500	CHOKE 80R/100MHZ SMD	1	
L15	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L16	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L17	0860,501	IND EMI FLTER 100PF SMD	1	
L18	0860,501	IND EMI FLTER 100PF SMD	1	
L19	0860,501	IND EMI FLTER 100PF SMD	1	
L20	0860,501	IND EMI FLTER 100PF SMD	1	
L21	0860,502	IND EMI FILTER 2N2 SMD	1	
L24	0860,502	IND EMI FILTER 2N2 SMD	1	
L25	0860,501	IND EMI FLTER 100PF SMD	1	
L26	0860,501	IND EMI FLTER 100PF SMD	1	
L27	0860,502	IND EMI FILTER 2N2 SMD	1	
L28	0860,502	IND EMI FILTER 2N2 SMD	1	
L29	0860,501	IND EMI FLTER 100PF SMD	1	
L30	0860,502	IND EMI FILTER 2N2 SMD	1	
L31	0860,501	IND EMI FLTER 100PF SMD	1	
L32	0860,502	IND EMI FILTER 2N2 SMD	1	
L33	0860,502	IND EMI FILTER 2N2 SMD	1	
L34	0860,502	IND EMI FILTER 2N2 SMD	1	
L35	0860,502	IND EMI FILTER 2N2 SMD	1	
L36	0860,502	IND EMI FILTER 2N2 SMD	1	
L37	0860,501	IND EMI FLTER 100PF SMD	1	
L38	0860,502	IND EMI FILTER 2N2 SMD	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
L39	0860,502	IND EMI FILTER 2N2 SMD	1	
L40	0860,501	IND EMI FLTER 100PF SMD	1	
L41	0860,502	IND EMI FILTER 2N2 SMD	1	
L42	0860,502	IND EMI FILTER 2N2 SMD	1	
L43	0860,502	IND EMI FILTER 2N2 SMD	1	
LK1	0804,007	CONR 3W WAFR SIL 2MM STR	1	
LK2	0804,009	CONR 9W WAFR SIL 2MM STR	1	
LK55				NOT FITTED
PL1	0800,297	CONRD 9WPLG RA PCB+RFI+L	1	
PL2	0804,004	CONR 16W STAKE 2ROW 2mmP	2	
PL3	0804,011	CONR 26W BOX HDR 2ROW 2MM	1	
PL4	0804,010	CONR 6W HDR SIL 2MM LK	1	
PL5	0804,000	CONR 6W BOX HDR 2ROW 2MM	1	
PL6	0804,001	CONR 10W BOX HDR 2ROW 2MM	1	
PL7	0804,005	CONR 10W WAFR 2ROW 2MM ST	1	
Q1	0778,212	VOLT REG 78L12 12V 8PSOIC	1	
Q2	0778,205	VOLT REG 5V UPWR TO92	1	
Q3	0784,849	TRANS BC849C NPN SOT23	1	
Q4	0784,859	TRANS BC859C PNP SOT23	1	
Q5	0784,859	TRANS BC859C PNP SOT23	1	
Q6	0784,849	TRANS BC849C NPN SOT23	1	
Q7	0784,849	TRANS BC849C NPN SOT23	1	
R1	0523,333	RES 33K SMD 5% 0W10 0805	1	
R2	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R3	0523,471	RES 470R SMD 5% 0W10 0805	1	
R4	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R5	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R6	0523,183	RES 18K SMD 5% 0W10 0805	1	
R7	0523,104	RES 100K SMD 5% 0W10 0805	1	
R8	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R9	0523,680	RES 68R SMD 5% 0W10 0805	1	
R10	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R11	0523,331	RES 330R SMD 5% 0W10 0805	1	
R12	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R13	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R14	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R15	0523,680	RES 68R SMD 5% 0W10 0805	1	
R16	0523,103	RES 10K SMD 5% 0W10 0805	1	
R17	0523,223	RES 22K SMD 5% 0W10 0805	1	
R18	0523,183	RES 18K SMD 5% 0W10 0805	1	
R19	0523,223	RES 22K SMD 5% 0W10 0805	1	
R20	0523,680	RES 68R SMD 5% 0W10 0805	1	
R21	0523,221	RES 220R SMD 5% 0W10 0805	1	
R22	0523,330	RES 33R SMD 5% 0W10 0805	1	
R23	0523,330	RES 33R SMD 5% 0W10 0805	1	
R24	0523,680	RES 68R SMD 5% 0W10 0805	1	
R25	0523,223	RES 22K SMD 5% 0W10 0805	1	
R26	0523,330	RES 33R SMD 5% 0W10 0805	1	
R27	0523,105	RES 1M0 SMD 5% 0W10 0805	1	
R28	0523,330	RES 33R SMD 5% 0W10 0805	1	
R29	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R30	0523,330	RES 33R SMD 5% 0W10 0805	1	
R31	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R32	0523,330	RES 33R SMD 5% 0W10 0805	1	
R33	0523,331	RES 330R SMD 5% 0W10 0805	1	
R34	0523,152	RES 1K5 SMD 5% 0W10 0805	1	
R35	0523,331	RES 330R SMD 5% 0W10 0805	1	
R36	0523,331	RES 330R SMD 5% 0W10 0805	1	
R37	0523,104	RES 100K SMD 5% 0W10 0805	1	
R38	0523,104	RES 100K SMD 5% 0W10 0805	1	
R39	0523,104	RES 100K SMD 5% 0W10 0805	1	
R40	0523,103	RES 10K SMD 5% 0W10 0805	1	
R41	0523,104	RES 100K SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R42	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R43	0523,330	RES 33R SMD 5% 0W10 0805	1	
R44	0523,330	RES 33R SMD 5% 0W10 0805	1	
R45	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R46	0523,561	RES 560R SMD 5% 0W10 0805	1	
R47	0523,100	RES 10R SMD 5% 0W10 0805	1	
R48	0523,330	RES 33R SMD 5% 0W10 0805	1	
R49	0523,680	RES 68R SMD 5% 0W10 0805	1	
R50	0523,680	RES 68R SMD 5% 0W10 0805	1	
R51	0523,680	RES 68R SMD 5% 0W10 0805	1	
R52	0523,680	RES 68R SMD 5% 0W10 0805	1	
R53	0523,680	RES 68R SMD 5% 0W10 0805	1	
R54	0523,680	RES 68R SMD 5% 0W10 0805	1	
R55	0523,680	RES 68R SMD 5% 0W10 0805	1	
R56	0523,680	RES 68R SMD 5% 0W10 0805	1	
R57	0523,680	RES 68R SMD 5% 0W10 0805	1	
R58	0523,680	RES 68R SMD 5% 0W10 0805	1	
R59	0523,680	RES 68R SMD 5% 0W10 0805	1	
R60	0523,680	RES 68R SMD 5% 0W10 0805	1	
R61	0523,680	RES 68R SMD 5% 0W10 0805	1	
R62	0523,680	RES 68R SMD 5% 0W10 0805	1	
R63	0523,680	RES 68R SMD 5% 0W10 0805	1	
R64	0523,680	RES 68R SMD 5% 0W10 0805	1	
R65	0523,680	RES 68R SMD 5% 0W10 0805	1	
R66	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R67	0523,330	RES 33R SMD 5% 0W10 0805	1	
R68	0523,473	RES 47K SMD 5% 0W10 0805	1	
R69	0523,473	RES 47K SMD 5% 0W10 0805	1	
R70	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R71	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R72	0523,330	RES 33R SMD 5% 0W10 0805	1	
R73	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R74	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R75	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R76	0523,473	RES 47K SMD 5% 0W10 0805	1	
R77	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R78	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R79	0523,330	RES 33R SMD 5% 0W10 0805	1	
R80	0523,183	RES 18K SMD 5% 0W10 0805	1	
R81	0523,330	RES 33R SMD 5% 0W10 0805	1	
R82	0523,100	RES 10R SMD 5% 0W10 0805	1	
R83	0523,330	RES 33R SMD 5% 0W10 0805	1	
R84	0523,221	RES 220R SMD 5% 0W10 0805	1	
R85	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R86	0523,331	RES 330R SMD 5% 0W10 0805	1	
R87	0523,680	RES 68R SMD 5% 0W10 0805	1	
R88	0523,561	RES 560R SMD 5% 0W10 0805	1	
R89	0523,103	RES 10K SMD 5% 0W10 0805	1	
R90	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R91	0523,330	RES 33R SMD 5% 0W10 0805	1	
R92	0523,183	RES 18K SMD 5% 0W10 0805	1	
R93	0523,223	RES 22K SMD 5% 0W10 0805	1	
R94	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R95	0523,105	RES 1M0 SMD 5% 0W10 0805	1	
R96	0523,330	RES 33R SMD 5% 0W10 0805	1	
R97	0523,183	RES 18K SMD 5% 0W10 0805	1	
R98	0523,330	RES 33R SMD 5% 0W10 0805	1	
R99	0523,223	RES 22K SMD 5% 0W10 0805	1	
R100	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R101	0523,330	RES 33R SMD 5% 0W10 0805	1	
R102	0509,001	RES 0R33 0W5 1% AXIAL	1	
R103	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R104	0509,001	RES 0R33 0W5 1% AXIAL	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R105	0523,331	RES 330R SMD 5% 0W10 0805	1	
R106	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R107	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R108	0523,100	RES 10R SMD 5% 0W10 0805	1	
R109	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R110	0523,331	RES 330R SMD 5% 0W10 0805	1	
R111	0523,103	RES 10K SMD 5% 0W10 0805	1	
R112	0523,330	RES 33R SMD 5% 0W10 0805	1	
R113	0523,103	RES 10K SMD 5% 0W10 0805	1	
R114	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R115	0523,680	RES 68R SMD 5% 0W10 0805	1	
R116	0523,680	RES 68R SMD 5% 0W10 0805	1	
R117	0523,680	RES 68R SMD 5% 0W10 0805	1	
R118	0523,680	RES 68R SMD 5% 0W10 0805	1	
R119	0523,680	RES 68R SMD 5% 0W10 0805	1	
R120	0523,680	RES 68R SMD 5% 0W10 0805	1	
R121	0523,680	RES 68R SMD 5% 0W10 0805	1	
R122	0523,680	RES 68R SMD 5% 0W10 0805	1	
R123	0523,680	RES 68R SMD 5% 0W10 0805	1	
R124	0523,680	RES 68R SMD 5% 0W10 0805	1	
R125	0523,680	RES 68R SMD 5% 0W10 0805	1	
R126	0523,680	RES 68R SMD 5% 0W10 0805	1	
R127	0523,680	RES 68R SMD 5% 0W10 0805	1	
R128	0523,680	RES 68R SMD 5% 0W10 0805	1	
R129	0523,220	RES 22R SMD 5% 0W10 0805	1	
R130	0523,220	RES 22R SMD 5% 0W10 0805	1	
R131	0523,220	RES 22R SMD 5% 0W10 0805	1	
R132	0523,220	RES 22R SMD 5% 0W10 0805	1	
R133	0523,220	RES 22R SMD 5% 0W10 0805	1	
R134	0523,331	RES 330R SMD 5% 0W10 0805	1	
R135	0523,103	RES 10K SMD 5% 0W10 0805	1	
R136	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R137	0523,680	RES 68R SMD 5% 0W10 0805	1	
R138	0523,331	RES 330R SMD 5% 0W10 0805	1	
R139	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R140	0523,330	RES 33R SMD 5% 0W10 0805	1	
R141	0523,330	RES 33R SMD 5% 0W10 0805	1	
R142	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R143	0523,103	RES 10K SMD 5% 0W10 0805	1	
R144	0523,331	RES 330R SMD 5% 0W10 0805	1	
R145	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R146	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R147	0523,332	RES 3K3 SMD 5% 0W10 0805	1	
R148	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R149	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R150	0523,330	RES 33R SMD 5% 0W10 0805	1	
R151	0523,330	RES 33R SMD 5% 0W10 0805	1	
R152	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R153	0523,330	RES 33R SMD 5% 0W10 0805	1	
R154	0523,330	RES 33R SMD 5% 0W10 0805	1	
R155	0523,103	RES 10K SMD 5% 0W10 0805	1	
R156	0523,330	RES 33R SMD 5% 0W10 0805	1	
R157	0523,330	RES 33R SMD 5% 0W10 0805	1	
R158	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R159	0523,330	RES 33R SMD 5% 0W10 0805	1	
R160	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R161	0523,330	RES 33R SMD 5% 0W10 0805	1	
R162	0523,330	RES 33R SMD 5% 0W10 0805	1	
R163	0523,330	RES 33R SMD 5% 0W10 0805	1	
R164	0523,103	RES 10K SMD 5% 0W10 0805	1	
R165	0523,330	RES 33R SMD 5% 0W10 0805	1	
R166	0523,330	RES 33R SMD 5% 0W10 0805	1	
R167	0523,330	RES 33R SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R168	0523,330	RES 33R SMD 5% 0W10 0805	1	
R169	0523,330	RES 33R SMD 5% 0W10 0805	1	
R170	0523,331	RES 330R SMD 5% 0W10 0805	1	
R171	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R172	0523,222	RES 2K2 SMD 5% 0W10 0805	1	
R173	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R174	0523,104	RES 100K SMD 5% 0W10 0805	1	
R175	0523,271	RES 270R SMD 5% 0W10 0805	1	
R176	0523,301	RES 300R SMD 5% 0W10 0805	1	
R177	0523,135	RES 1M3 SMD 5% 0W10 0805	1	
R178	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R179	0523,101	RES 100R SMD 5% 0W10 0805	1	
R180	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R181	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R182	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R183	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R184	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R185	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R186	0523,222	RES 2K2 SMD 5% 0W10 0805	1	
R187	0523,222	RES 2K2 SMD 5% 0W10 0805	1	
R188	0523,221	RES 220R SMD 5% 0W10 0805	1	
R189	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R190	0523,223	RES 22K SMD 5% 0W10 0805	1	
R191	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R192	0523,101	RES 100R SMD 5% 0W10 0805	1	
R193	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R194	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R195	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R196	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R197	0523,105	RES 1M0 SMD 5% 0W10 0805	1	
R198	0523,332	RES 3K3 SMD 5% 0W10 0805	1	
R199	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R200	0522,425	RES 18K2 SMD 1% 0W25 1206	1	
R201	0523,332	RES 3K3 SMD 5% 0W10 0805	1	
R202	0523,103	RES 10K SMD 5% 0W10 0805	1	
R203	0522,317	RES 1K50 SMD 1% 0W25 1206	1	
R204	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R205	0522,380	RES 6K81 SMD 1% 0W25 1206	1	
R206	0522,450	RES 33K2 SMD 1% 0W25 1206	1	
R207	0523,101	RES 100R SMD 5% 0W10 0805	1	
R208	0523,271	RES 270R SMD 5% 0W10 0805	1	
R209	0522,500	RES 100K SMD 1% 0W25 1206	1	
R210	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R211	0523,271	RES 270R SMD 5% 0W10 0805	1	
R212	0522,558	RES 402K SMD 1% 0W25 1206	1	
R213	0523,680	RES 68R SMD 5% 0W10 0805	1	
R214	0523,104	RES 100K SMD 5% 0W10 0805	1	
R215	0525,202	RES 2K0 SMD .1% 0W1 1206	1	
R216	0525,152	RES 1K5 SMD .1% 0W1 1206	1	
R217	0525,163	RES 16K SMD .1% 0W1 1206	1	
R218	0523,823	RES 82K SMD 5% 0W10 0805	1	
R219	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R220	0523,103	RES 10K SMD 5% 0W10 0805	1	
R221	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R222	0523,183	RES 18K SMD 5% 0W10 0805	1	
R223	0523,471	RES 470R SMD 5% 0W10 0805	1	
R224	0523,103	RES 10K SMD 5% 0W10 0805	1	
R225	0523,103	RES 10K SMD 5% 0W10 0805	1	
R226	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R227	0523,680	RES 68R SMD 5% 0W10 0805	1	
R228	0523,680	RES 68R SMD 5% 0W10 0805	1	
R229	0523,680	RES 68R SMD 5% 0W10 0805	1	
R230	0523,680	RES 68R SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R231	0523,680	RES 68R SMD 5% 0W10 0805	1	
R232	0523,103	RES 10K SMD 5% 0W10 0805	1	
R503	0523,680	RES 68R SMD 5% 0W10 0805	1	
R504	0523,680	RES 68R SMD 5% 0W10 0805	1	
R505	0523,680	RES 68R SMD 5% 0W10 0805	1	
R506	0523,680	RES 68R SMD 5% 0W10 0805	1	
R507	0523,680	RES 68R SMD 5% 0W10 0805	1	
R508	0523,680	RES 68R SMD 5% 0W10 0805	1	
R509	0523,680	RES 68R SMD 5% 0W10 0805	1	
R510	0523,680	RES 68R SMD 5% 0W10 0805	1	
R511	0523,680	RES 68R SMD 5% 0W10 0805	1	
R512	0523,680	RES 68R SMD 5% 0W10 0805	1	
R513	0523,680	RES 68R SMD 5% 0W10 0805	1	
R514	0523,680	RES 68R SMD 5% 0W10 0805	1	
R515	0523,680	RES 68R SMD 5% 0W10 0805	1	
R516	0523,680	RES 68R SMD 5% 0W10 0805	1	
R517	0523,680	RES 68R SMD 5% 0W10 0805	1	
R518	0523,680	RES 68R SMD 5% 0W10 0805	1	
R519	0523,104	RES 100K SMD 5% 0W10 0805	1	
R520	0523,104	RES 100K SMD 5% 0W10 0805	1	
R521	0523,104	RES 100K SMD 5% 0W10 0805	1	
R522	0523,104	RES 100K SMD 5% 0W10 0805	1	
R523	0523,104	RES 100K SMD 5% 0W10 0805	1	
R524	0523,104	RES 100K SMD 5% 0W10 0805	1	
R525	0523,104	RES 100K SMD 5% 0W10 0805	1	
R526	0523,104	RES 100K SMD 5% 0W10 0805	1	
R527	0523,104	RES 100K SMD 5% 0W10 0805	1	
R528	0523,104	RES 100K SMD 5% 0W10 0805	1	
R529	0523,104	RES 100K SMD 5% 0W10 0805	1	
R549	0523,104	RES 100K SMD 5% 0W10 0805	1	
R551	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R552	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
SK1	0800,925	CONR 9W MINDIN RAPCB MRFI	1	
SK2	0800,645	CONR 3,5MM RA PCB JKSKT	1	
SK3	0801,203	CONR 20W FPC 1MMP ST ZIF	1	
SK4	0801,203	CONR 20W FPC 1MMP ST ZIF	1	
SK5	0801,206	CONR 26W 1,25 RA FPC ZIF	1	
SK6	0800,995	CONRD 15WSKT RA HD+RFI+L	1	
SK7	0194,008	VIDEO HYBRID 15P	1	
SK10	0898,005	CONRD 25WSKT RA PCB+RF+L	1	
SK11	0801,204	CONR 8W 1,25MM ST CIC ZIF	1	
SK12	0801,205	CONR 20W 1,25 ST CIC ZIF	1	
SK15	0800,923	CONR 6W MINDIN RAPCB MRFI	1	
SW1	0805,709	SW 1P MOM PTM P/B RA PCB	1	
SW2	0805,125	SW SP 3W CO ROTARY SMD	1	
SW3	0805,126	SW SPCO ROTARY SMD	1	
X1	0820,243	XTAL 24MHZ HC49 5,08MMH	1	
X2	0821,327	XTAL 32.768KHZ CC 0.05P	1	
X3	0820,253	XTAL 25.175MHZ HC49 5,08H	1	
X4	0820,243	XTAL 24MHZ HC49 5,08MMH	1	
X5	0820,363	XTAL OSC 36MHZ CMOS 8P PL	1	
X6	0820,041	XTAL 4.194304M HC49 5,08H	1	
Z1	0796,102	DIODE 3V9 ZNR 0W3 SOT23	1	
Z2	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z3	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z4	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z5	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z6	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z7	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z8	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z9	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z10	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z11	0796,103	DIODE 5V1 ZNR 0W3 SOT23	1	
Z12	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	

A4 4M + 60MHD final assembly parts list, issue 4

ITEM	PART No.	DESCRIPTION	QTY	Remarks
	0090,260/A	Final Assy Drg		1 Per Batch
	0190,009	Perth Display Unit Assy	1	
	0190,011	Perth UK Keyboard Assy	1	
	0490,043	Perth Base Label	1	
	0290,063	Floppy Disc Flexy Cable	1	
	0190,067	H/D Ribbon Cable Assy	1	
	0190,074	ON/OFF/Battery Cable Assy	1	
	0290,075	Rear Wall RFI Shield	1	
	0290,076	Main PCB Insulation Sheet	1	
	0290,077	Clamp Plate	1	
	0190,083	DC/DC Convertor PCB Assy	1	
	0190,084	H/D Bracket (Conner)	1	
	0190,085	K/B Rear Edge Carrier	1	
	0190,094	DC Inlet Cable Assembly	1	
	0190,095	Battery LCD Cable Assy	1	
	0290,097	Battery LCD Perspex Windw	1	
	0290,100	Nut M3 Collared captive	3	
	0190,103	Rear Wall RFI Strip	1	
	0290,104	Keyboard Support Collar	3	
	0190,109	Scw M3x4 Pan Head Posi Sp	3	Use on Item 48
	0190,110	Scw 3x8 TC Pan Head PosiS	5	Use on Items 17, 48
	0190,112	Scw 3x35 TC Pan Posi Spec	3	Use on Items 6,41
	0290,114	K/B Rear Edge RFI Strip	1	
	0190,115	Floppy Disc Drive Bezel	1	
	0290,117	Battery Status LCD	1	
	0290,118	Floppy D/D RFI Plate	1	
	0290,119	Battery LCD Insulator	1	
	0190,120	Side Drop Flap	1	
	0190,121	Case Lower Sliding Insert	1	
	0190,122	Case Lower (TA/Acorn)	1	
	0190,125	Rear Drop Flap (TA/Acorn)	1	
	0290,135	Foam Strip (Long) 15mm		
	0290,140	DC/DC Con-H/D RFI Shield	1	
	0190,142	Scw with Washer M3x5	4	Use on Item 73
	0190,145	Rear Wall	1	
	0190,260	Perth (4M) Main PCB Assy	1	
	0800,999	Conrd 4-40UNC Scwlk Stpd	8	
	0800,997	Wshr 4-40UNC Int-Sprf SnP	2	Use on Item 22
	0800,998	Nut 4-40UNC Z&P	2	Use on Item 22
	0805,909	SW SPST DC 2A Roc Snp	1	Use on Item 14
	0882,121	Scw M3x6 Pan Hd Posi	4	Use on Items 19,74
	0882,717	Scw 3x6mm Pan Posi PLST45	1	Use on Item 19
	0895,082	Adh Pad Insulator	4	Use on Item 16
	0907,008	Tape Plstc Blk Insu SFAD 20mm		Use on Items 26,48
	0912,018	Floppy Drive 2MB 3.518mm	1	
	0912,025	Wini Drive 60MB 2.5 IDE	1	
	0940,004	Adh Scw-Lock 222 A/R		Use on Items 56,58

A4 Econet PCB assembly parts list, issue 1

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0290,005	BARE PCB		1
2	0190,005/A	PCB ASSEMBLY DWG		1 PER BATCH
3	0190,005/C	PCB CIRCUIT DIAGRAM		1 PER BATCH
16	0902,012	LABEL SERIAL NO SA 40x10mm	1	
C1	0692,333	CPCTR 33N CML 20% 805	1	
C2	0692,333	CPCTR 33N CML 20% 805	1	
C4	0647,002	CPCTR 47U ALEC 16V SMD	1	
C5	0681,100	CPCTR 47U TANT SMD	1	
C6	0681,101	CPCTR 10U TANT SMD 16V	1	
C7	0691,222	CPCTR 2N2 CML 10% 805	1	
C8	0692,333	CPCTR 33N CML 20% 805	1	
C9	0692,103	CPCTR 10N CML 20% 805	1	
C10	0692,333	CPCTR 33N CML 20% 805	1	
C11	0692,333	CPCTR 33N CML 20% 805	1	
C12	0692,333	CPCTR 33N CML 20% 805	1	
C13	0692,333	CPCTR 33N CML 20% 805	1	
C14	0692,333	CPCTR 33N CML 20% 805	1	
C15	0647,002	CPCTR 47U ALEC 16V SMD	1	
C16	0647,002	CPCTR 47U ALEC 16V SMD	1	
IC1	0732,635	IC 26LS30 RS422/3 DR SOIC	1	
IC2	0764,123	IC 74LS123 TTL 16P SOIC	1	
IC3	0771,319	IC LM319 DUAL COMP 14SOIC	1	
IC4	0771,319	IC LM319 DUAL COMP 14SOIC	1	
IC5	0706,855	IC 68B54 ADLC 2MHZ 28PLCC	1	
IC6	0761,132	IC 74HC132 CMOS 14P SOIC	1	
IC7	0761,244	IC 74HC244 CMOS 20P SOIC	1	
IC8	0762,245	IC 74HCT245 CMOS 20P SOIC	1	
PL1	0804,003	CONR 26W BOX HDR 2R 2MMRA	1	
Q1	0784,018	TRANS BCX18 PNP SOT23	1	
R1	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R2	0523,155	RES 1M5 SMD 5% 0W10 0805	1	
R3	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R4	0523,155	RES 1M5 SMD 5% 0W10 0805	1	
R5	0524,103	RES 10K SMD 2% 0W1 0805	1	
R6	0523,155	RES 1M5 SMD 5% 0W10 0805	1	
R7	0524,103	RES 10K SMD 2% 0W1 0805	1	
R8	0524,103	RES 10K SMD 2% 0W1 0805	1	
R9	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R10	0523,561	RES 560R SMD 5% 0W10 0805	1	
R11	0523,224	RES 220K SMD 5% 0W10 0805	1	
R12	0523,393	RES 39K SMD 5% 0W10 0805	1	
R13	0524,563	RES 56K SMD 2% 0W1 0805	1	
R14	0524,152	RES 1K5 SMD 2% 0W1 0805	1	
R15	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R16	0524,563	RES 56K SMD 2% 0W1 0805	1	
R17	0524,563	RES 56K SMD 2% 0W1 0805	1	
R18	0524,104	RES 100K SMD 2% 0W1 0805	1	
R19	0524,563	RES 56K SMD 2% 0W1 0805	1	
R20	0524,102	RES 1K0 SMD 2% 0W1 0805	1	
R21	0524,104	RES 100K SMD 2% 0W1 0805	1	
R22	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R23	0524,103	RES 10K SMD 2% 0W1 0805	1	
R24	0524,104	RES 100K SMD 2% 0W1 0805	1	
R25	0524,104	RES 100K SMD 2% 0W1 0805	1	
R26	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R27	0521,472	RES 4K7 SMD 5% 0W25 1206	1	
R28	0521,472	RES 4K7 SMD 5% 0W25 1206	1	
SK1	0800,924	SKT 5W MINDIN RA PCB RFI	1	

A4 display assembly parts list, issue 2

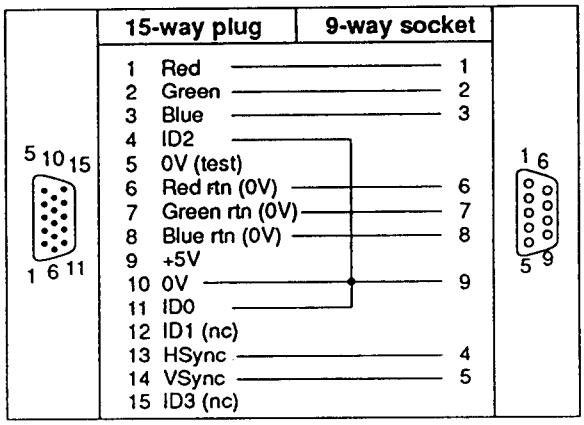
ITEM	PART No.	DESCRIPTION	QTY	Remarks
	0190,009/A	Assembly Drg		1 Per Batch
	0490,041	Perth Acorn Logo Label	1	
	0190,086	Upgrade Cover {TA/Acorn}	1	
	0190,088	Case Upper {TA/Acorn}	1	
	0290,098	Hinge Pin {Short}	1	
	0290,099	Hinge Pin {Long}	1	
	0290,101	Lid Screw Cover	2	
	0290,102	Lid Hinge Cam Nut	2	
	0290,105	Lid Catch Release Button	2	
	0290,106	Lid Catch	2	
	0290,108	Thumbwheel	2	
	0190,111	SCW 2.2x6 TC Pan Posi	2	Use on Item 17
	0190,113	SCW 2.2x4.5 TC Pan Posi	2	Use on Items 20,21
	0190,123	Display Carrier{TA/Acorn}	1	
	0190,124	Display Frame {TA/Acorn}	1	
	0290,126	B/L Control PCB Insul Sht	1	
	0290,127	Insulating Washer	2	
	0190,128	B/L Control PCB Assy	1	
	0190,129	Speaker PCB Assy	1	
	0290,175	Spring Clip	2	
	0190,133	Control/Speaker PCB Cable	1	
	0290,134	Display Foam Strip{Short}	2	
	0290,135	Display Foam Strip {Long}	2	
	0290,136	Display Central Foam Pad	1	
	0290,137	Hinge Pin Spacer {Short}	1	
	0290,138	Hinge Pin Spacer {Long}	1	
	0290,139	Main Insulator Sheet	1	
	0290,141	Speaker PCB Insulator Sht	1	
	0290,143	Wshr Hinge Pin	2	
	0190,158	Lamp & Diffuser Assy	1	
	0290,162	Display Frame Insul Sht	1	
	0290,176	Insulating Washer	2	
	0870,224	Cbl 20W FlatFlex 1mmP 88L	1	
	0870,226	Cbl 20W FlatFlex 1mmP 98L	1	
	0895,083	Adh Pad Foam SS 5mm Thk	1	
	0913,002	LCD Mono VGA Transmissive	1	
	0940,009	Grease Contact Treatment A/R		Use on Items 5,16

Appendix A – Monitor adaptor cables

This appendix describes how to make adaptor cables for monitors not supplied with a 15-way VGA connector.

Adaptor type 1

The cable supplied with some Multiscan monitors is terminated at the computer end with a 9-way D-type plug. You need a standard 15-way plug to 9-way socket adaptor:

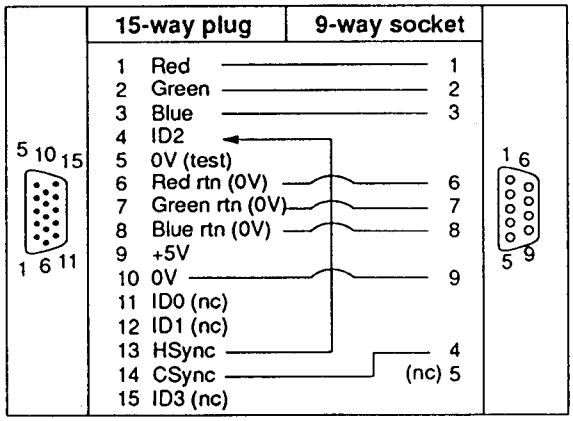


Note: The ID[0] to 0V connection will make the monitor type 3 modes available and the computer will generate separate sync signals.

Most Multiscan monitors are now being designed to be VGA-compatible and will work satisfactorily when driven with separate horizontal and vertical sync signals.

Adaptor type 2

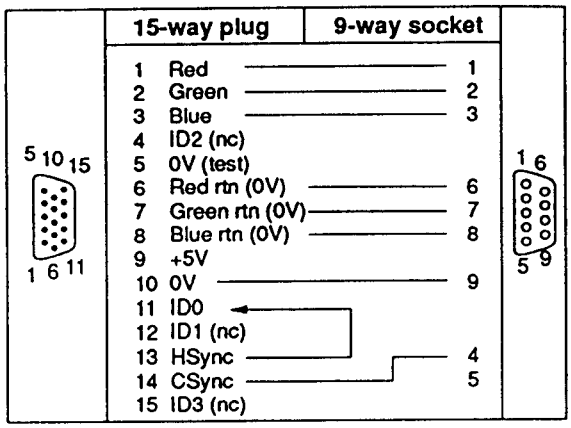
The cable supplied with some Multiscan monitors requiring composite sync is terminated at the computer end with a 9 pin D-type plug. You need a 15-way plug to 9-way socket adaptor:



Note: The HSYNC to ID[2] connection will make the monitor type 1 modes available and the computer will generate a composite sync signal.

Adaptor type 3

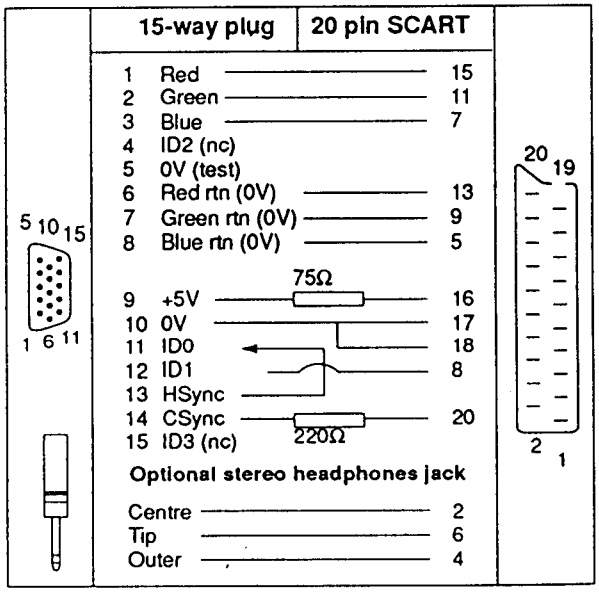
The cable supplied with some TV-type monitors is terminated at the computer end with a 9 pin D-type plug. You need a 15-way plug to 9-way socket adaptor:



Note: The HSYNC to ID[0] connection will make the monitor type 0 modes available and the computer will generate a composite sync signal.

Cable type 4

You need to make this cable to use with televisions and TV-type monitors using a SCART input socket:

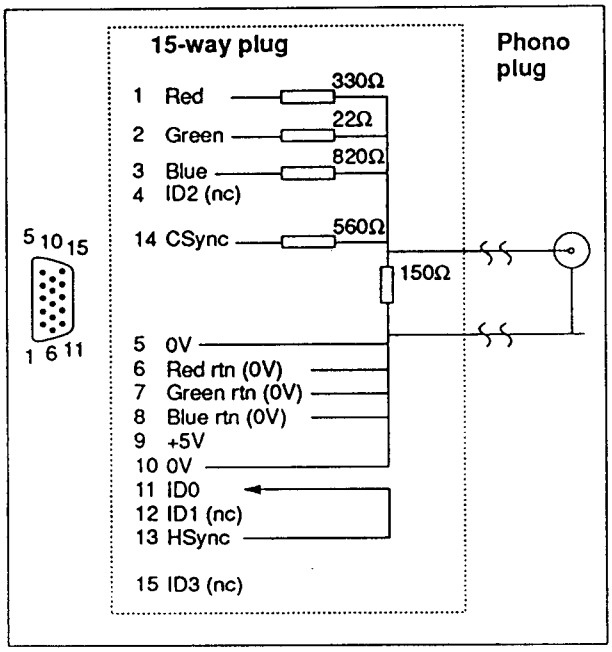


The 220Ω resistor results in a CSYNC signal of approximately 1V peak on pin 20 of the SCART connector. The 75Ω resistor results in a blanking signal of approximately 2.5V dc on pin 16 of the SCART connector.

Cable type 5

You need to make this cable to use with monochrome monitors which have a phono input socket. You need a 15-way plug to phono socket adaptor with resistors, to mix the separate red, green and blue signals into a composite monochrome signal (you can fit these components into a 15-way connector shell).

You need to make an adaptor cable that has a 15-way D-type plug on one end, and a phono plug on the other. The connections you need to make are as follows:



Note: The HSYNC to ID[0] connection will make the monitor type 0 modes available and the computer will generate a composite sync signal.

Appendix B – Expansion bay

The expansion bay is provided for low-power miniature expansion cards. These cards are mounted in a lid moulding that clips into the top of the case. The interface connector has a limited set of signals, due to space constraints, and has been designed specifically to support the A4 Econet module. It should not be regarded as a general purpose expansion slot.

Interface

The interface connector PL3 provides the select lines $\overline{S2}$ and $\overline{S4}$. These are IOC-controlled memory-mapped peripheral select lines which allow programmable slow, medium, fast or synchronous cycles. See *I/O system* on page 1-2 for address details and IOC data sheet (available separately – see page iv) for timing information.

Details of other signals

LA[2:5]
Addressing 16 register locations.

CLK2
2MHz clock derived from the main I/O clock. When programmed for a synchronous cycle this signal can be used as ECLK for communications with 6800 peripherals (see the Econet circuit diagram in *Appendix C – Engineering drawings*).

$\overline{WBE}$
Write buffer enable. This signal, generated by IOC, enables the on board write buffers during an IOC controlled cycle and is used as a read/write strobe on the Econet upgrade. (See IOC data sheet for timing details)

$\overline{EFIQ}$
Active low FIQ used for Econet upgrade. Appears as bit 2 FIQ status register 3200030. This signal has a 4k7 resistive pull-up on the main PCB.

$\overline{PIRQ}$
Active low IRQ, appears as bit 5 in the IOC IRQ status register B address 3200020. This signal has a 4k7 resistive pull-up on the main PCB.

$\overline{PWE}$ and $\overline{PRE}$
Podule read write strobes used to manipulate data during programmed I/O cycles. (See IOC data sheet for timing details).

$\overline{RST}$
System reset. Open drain signal driven by IOC at power up and by IOEB when the reset button is pressed. This signal can be driven by the expansion card. The pulse width should be at least 250ms. Output drivers should be able to sink at least 6mA (1k2 pull-up plus four LS TTL gate input loads.)

BD[0:7]
It is recommended that these lines are buffered prior to use on an expansion card (see below).

$\overline{ECON}$
Power control signal. This signal is controlled by register LICR (address 302C030) bit 0 in the LC ASIC. By programming this bit to a logic 1, the $\overline{ECON}$ signal goes low (this bit is set to logic 1 after reset).

Power available

It is recommended that the expansion card draws no more than 200mA @ 5V continuous, to avoid excessive heating within the A4 unit. It is also recommended that peak currents are limited to 400mA. This is particularly important at machine power-on when the charger unit may have to supply current to charge a flat battery, spin up discs etc.

Using the power control signal

It is strongly recommended that when not in use the expansion card is powered down to conserve battery life. To ensure that the expansion circuitry is protected when powered down, isolation buffers are needed. A scheme for isolating the Econet circuitry and switching the 5V rail is shown on the Econet circuit diagram in *Appendix C – Engineering drawings*.

Mechanical issues

Figure B.1 shows the outline of the Econet module PCB. This outline should be followed to ensure a fit with the cover moulding (Acorn part number 0191,087/T).

Figure B.2 shows the insulation sheet (Acorn part number 0290,062) that needs to be provided between the PCB and the lid assembly.

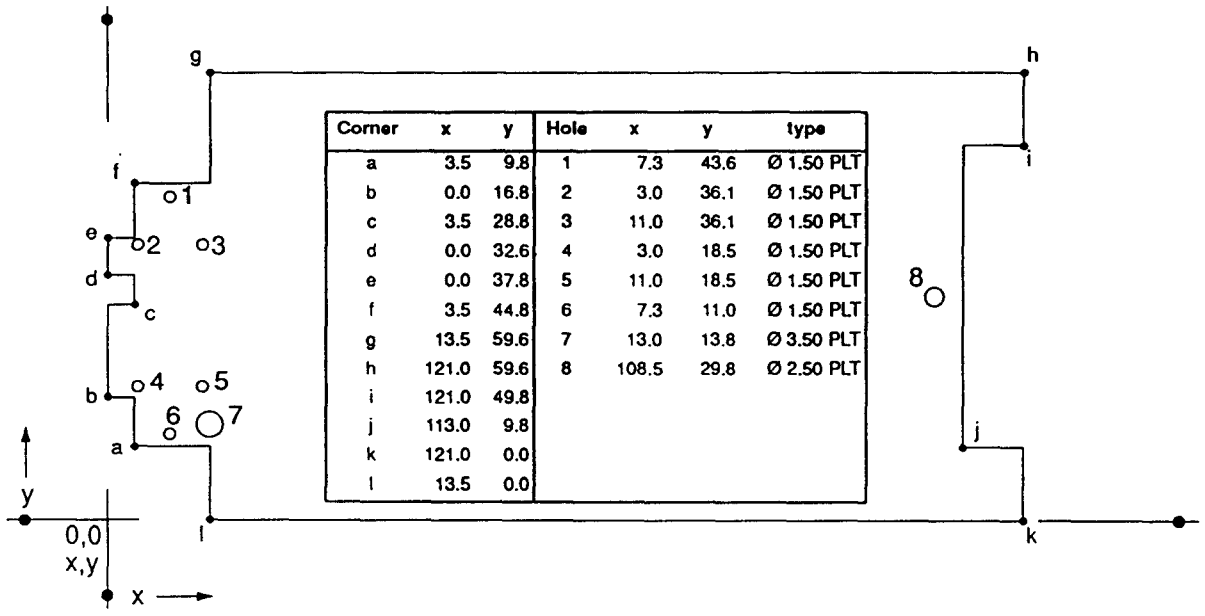
Connector information

The internal Econet upgrade cable (Acorn part number 0190,078/A) uses two 26-way connectors. For the pin out of the internal connector, see *Plugs* on page 1-26. The 5-pin mini-DIN to 5-pin DIN Econet lead (2m) is Acorn part number 0190,068/T.

PART No.	DESCRIPTION	QTY
0804,202	CONR 26W SKT HSNG 2mmFREE	2
0805,250	CONR 1W CRMP SKT 24-28AWG	52
0870141	WIRE 28AWG PVC UL1007	2100mm
0880,043	RUBBER SLEEVING	15mm

Figure B.1: Outline of Econet Module PCB

Note:
This diagram is abstracted from Acorn drawing No. 0290,005/D-02. All dimensions in mm. The hole numbered 1 to 6 are provided for the fitment of an RFI shield for the connector.

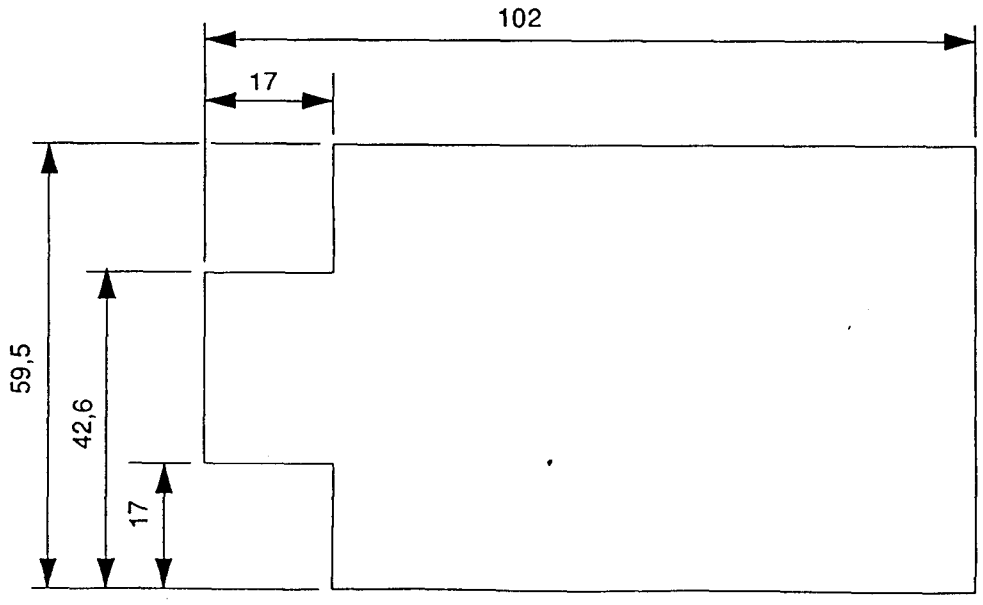


Corner	x	y
a	3.5	9.8
b	0.0	16.8
c	3.5	28.8
d	0.0	32.6
e	0.0	37.8
f	3.5	44.8
g	13.5	59.6
h	121.0	59.6
i	121.0	49.8
j	113.0	9.8
k	121.0	0.0
l	13.5	0.0

Hole	x	y	type
1	7.3	43.6	Ø 1.50 PLT
2	3.0	36.1	Ø 1.50 PLT
3	11.0	36.1	Ø 1.50 PLT
4	3.0	18.5	Ø 1.50 PLT
5	11.0	18.5	Ø 1.50 PLT
6	7.3	11.0	Ø 1.50 PLT
7	13.0	13.8	Ø 3.50 PLT
8	108.5	29.8	Ø 2.50 PLT

Figure B.2: Econet Insulation sheet

Note:
This diagram is abstracted from Acorn drawing No. 0290,062-02. All dimensions in mm. Material to Acorn Component Spec. 0906,004 (PETP insulating sheet 0.127mm thick).



Appendix C – Engineering drawings

- Final assembly drawings (base and display)
- Main PCB circuit diagram
- DC/DC convertor circuit diagram
- BacklightDC control board circuit diagram
- Speaker board circuit diagram
- Econet PCB circuit diagram

Reader's Comment Form

Acorn A4 Technical Reference Manual

We would greatly appreciate your comments about this Manual, which will be taken into account for the next issue:

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