Acorn Computers Ltd - Science and Industry Division

Technical Description and Service Manual

Acorn Cambridge 32016 Co-Processor

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Issue: Issue 1.

Release History: Issue C - Fault finding/Test program.
Issue B - 2nd Draft
Issue A - 1st Draft

Reference No: 0410,000

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Introduction

Nature and Purpose of the Manual

The main purpose of this manual is to provide technical information about the Acorn Cambridge 32016 Co-processor to the BBC Microcomputer system.

The manual is aimed at technical service staff and includes an outline technical specification and a detailed description of the operation of the circuit. Information is also given about how to upgrade the circuit and the purpose of the various links on the board. Some guidance is also provided about fault-finding and servicing.

Sales Order Code

The Acorn Cambridge 32016 Co-processor has sales order code : ANC05

Notation

¦	= Active low signal (eg. ¦CAS)
LSB	= A0,D0 etc.
MSB	= A23,D15 etc.
Word	= two bytes = 16 bits
Double	= four bytes = 32 bits
Quad	= eight bytes = 64 bits
NYA	= Not yet available
RSVD	= Reserved for future (Acorn) use
HHHHHH	= Hex (Hexadecimal notation)
BBBBBB	= Bin (Binary notation)

References to IC numbers and signal names refer to issue 2 of Acorn Drawing number 0110,000/C. A photo-reduced copy of which should be attatched to this document. Where conflicts arise in the documentation, the logic diagram should be assumed correct.

Mains power

WARNING: THE COMPUTER MUST BE EARTHED

IMPORTANT: The wires in the mains lead for the unit are coloured in accordance with the following code:

GREEN & YELLOW - EARTH

BLUE - NEUTRAL

BROWN - LIVE

If the socket outlet available is not suitable for the plug supplied, the plug should be cut off and the appropriate plug fitted and wired as above. As the colours of the wires may not correspond with the coloured markings identifying the terminals in your plug proceed as follows:

The wire which is coloured green and yellow must be connected to the terminal in the plug which is marked by the letter E, or by the safety earth symbol, or coloured either green or green and yellow.

The wire which is coloured blue must be connected to the terminal which is marked by the letter N, or coloured black.

The wire which is coloured brown must be connected to the terminal which is marked by the letter L, or coloured red.

The moulded plug which was cut off must be disposed of carefully as it would be a potential shock hazard if it were to be plugged in with the cut off end of mains cord exposed.

The moulded plug must be used with the fuse and fuse carrier firmly in place. The fuse carrier is of the same basic colour as the coloured insert in the base of the plug. Different manufacturers plugs and fuse carriers are not interchangeable.

In the event of the fuse blowing, it should be replaced, after clearing any faults with a 3 amp fuse that is approved to BS1362.

Do not use the unit in conditions of extreme heat, cold, humidity or dust or in places subject to vibration. Do not block the ventilation slots at the rear of the unit and ensure that no foreign objects are inserted through any openings in the case.

Hardware Technical Specification

Acorn document No. 0310,000 is a formal specification for the 32016 Co-processor.

Summary

The 32016 Co-processor is a "second processor" as described in the BBC Microcomputer user guide.

The circuit is based around the National Semiconductors 32016 series of processors and support devices which together provide a performance comparable with modern mini-computers. The circuit has been designed to allow operation at a processor clock rate of 10Mhz, when using memory devices with a 150nS access time. The actual clock rate will depend on the which National parts have been installed, probably 6 Mhz. The socketed memory array can accept either 64K or 256K bit DRAMs and this allows the memory to be field upgraded to 1 M Byte.

Packaging

The Acorn Cambridge 32016 Co-processor is supplied in a two part moulded polystyrene packing which is further packaged within a cardboard sleeve. A mains lead and plug is packed with the 32016 Co-processor. The packaging should be kept intact in case it becomes necessary to transport the unit at a later date.

Mechanical assembly of case

Removing the lid

WARNING: DO NOT REMOVE THE LID WITH THE MAINS POWER CONNECTED.

The lid of the Co-processor may be removed after undoing three fixing screws, two on the rear panel and one underneath. When reassembling, press the lid down at the rear whilst tightening the two rear fixing screws. Take care not to lose the two spire clips pushed onto the case lid, into which the rear fixing screws locate.

Inside the unit are two sub-assemblies, the power supply unit, and main printed circuit board.

Printed circuit - Removal

To remove the printed circuit board: remove the TUBE ribbon cable from the socket on the printed circuit board and detatch the push on power supply connectors; undo the six self-tapping screws that hold the board to the case bottom and lift clear.

WARNING: THE PRINTED CIRCUIT BOARD CONTAINS DEVICES WHICH CAN BE DAMAGED BY STATIC ELECTRICITY.

Power supply - Removal

To remove the power supply: detatch the mains live and neutral spade connectors from the rear of the mains switch; remove the self-tapping screw that secures the earth lead to the printed circuit board; detatch the push on power supply connectors from the printed circuit board; remove the six screws that hold the power supply to the bottom of the case and lift clear. On reassembly ensure that the correct screws are used.

General reassembly

To reassemble the Co-processor simply reverse the removal process.

CAUTION: BEFORE SWITCHING ON CHECK THE POLARITY OF THE 5V POWER SUPPLY TO THE PRINTED CIRCUIT BOARD.

The output from the power supply is colour coded:

5V - RED

0V - BLACK

If in doubt check with a voltmeter before connection as reverse polarity will destroy the components on the circuit board.

Outline circuit description

Main Components

A block diagram of the circuit is shown in Fig.1.

A number of main component blocks can be identified, these are :

Central processor unit	(CPU)	NS32016
Memory Management unit	(MMU)	NS32082
Timing and Control unit	(TCU)	NS32201
Floating Point unit	(FPU)	NS32081
Tube (R)		
Dynamic Memory array		64K/256K bit DRAMs
EPROM		2 off 16K*8

The main bus connecting these components together is the AD bus, this is a bidirectional multiplexed address/data bus.

The CPU is responsible for instruction fetch, decode, operand fetch and the execution of integer arithmetic. Floating point instructions together with the required operands are passed to the FPU for execution.

If the system has an MMU installed, Virtual addresses generated by the processor are intercepted by the MMU and mapped into Physical addresses before being used to access the memory.

The TCU provides a number of system clocks at half the crystal frequency. In addition it controls memory access cycles in conjunction with some additional TTL based circuitry.

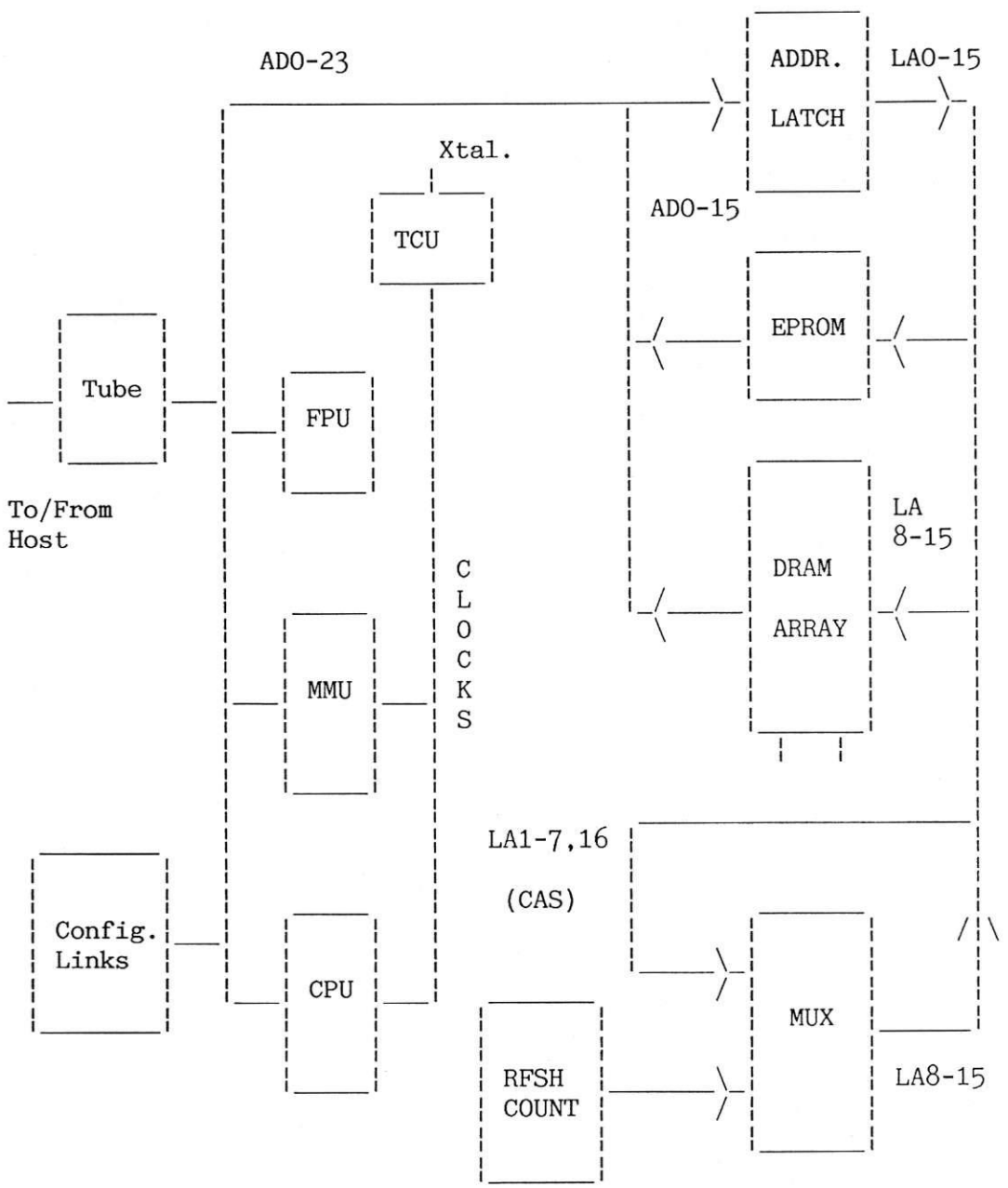
The TUBE (R) is a communications channel to the BBC Microcomputer system which acts as host or I/O processor. Data passes through the tube under program control0. An interrupt scheme is used on the 32016 side of the TUBE and polling is used on the Host side.

The socketed memory array is organised as two 1/4 M WORD sections. Each section is further divided into low and high byte banks.

The Configuration links are read by software and indicate the presence or absence of an FPU or MMU.

The EPROMs contain PANDORA. This code is responsible for initialisation on power-up and Break, and allows programs running on the 32016 Co-processor access to the BBC operating system and hardware. In practice all access to the BBC should be through PANOS, the Acorn operating system for 32016 based products.

FIG.1. 32016 CO-PROCESSOR BLOCK DIAGRAM



Detailed Circuit Description

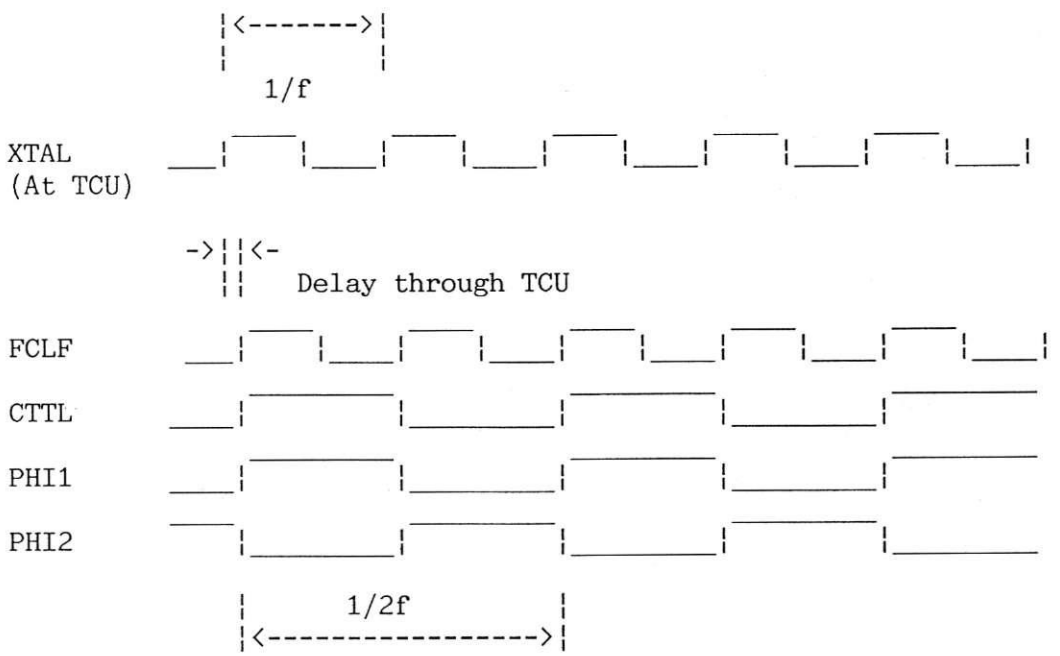
Refer to the logic diagram where necessary.

Clock scheme

The NS32201 Timing and Control unit produces a two phase MOS compatable clock (PHI1 and PHI2). These are used internally by the NS32000 family only. For general use throughout the remainder of the circuit the TCU provides CTTL which is a TTL compatable replica of PHI1 clock. All the above mentioned clocks run at half the crystal frequency. See Fig.2.

In order to reduce the probability of syncronisation failure occuring the crystal oscillator input to the TCU is paused (low) if both the host BBC Micro. and the 32016 access the tube simultaneously.

FIG.2. CLOCK SCHEME



Reset and Booting

Pressing BREAK on the keyboard causes a reset to occur in the host processor, this causes ¦HRST on the host side of the Tube to go low and this in turn causes ¦PRST on the 32016 side. ¦PRST is connected to the TCU reset in (¦RSTI). The TCU produces a system reset (¦RSTO) and it is this signal that resets the 32000 series devices.

During the reset recovery sequence (BOOTING) the CPU starts execution at location Hex 000000 (Zero), however it also expects to find a module table at location zero during program execution. This causes a problem as this first instruction must be held in EPROM and the module table must be in RAM. The problem has been solved using a technique known as "RAM-FLIP". During BOOTING the address decoding logic causes the EPROMs to appear at multiple locations including zero and the RAM is disabled. The first instruction held in EPROM at Hex 0000 is an unconditional branch into a high order copy of the EPROM (Typically address Hex F00010). Execution continues with a Write instruction (to no particular address) and this causes the address decoding logic to switch out low order copies of the EPROMs and enable the RAM.

The BOOTING sequence is controlled by an S-R latch formed by two cross-coupled NAND gates (IC15). The output ¦BOOTING is set low by a reset from the TUBE (¦PRST) and reset high by ¦WR. ¦BOOTING low forces the EPROM chip select (¦ROMCS) active causing the EPROM to respond to all addresses (ie it replicates at 16k word intervals)

Address map

The address map is not fully decoded which means that some devices (ie the TUBE) could be addressed at more than one location. The address map is illustrated in Fig.3. Software must only access devices at the addresses shown below.

Address map - during Booting

See Fig.3.a

The EPROMs replicate from address Hex 000000 to Hex FFFFFF at 32k byte intervals but are only addressed at:

Hex 000000 (One instruction during start-up)
and Hex F00000

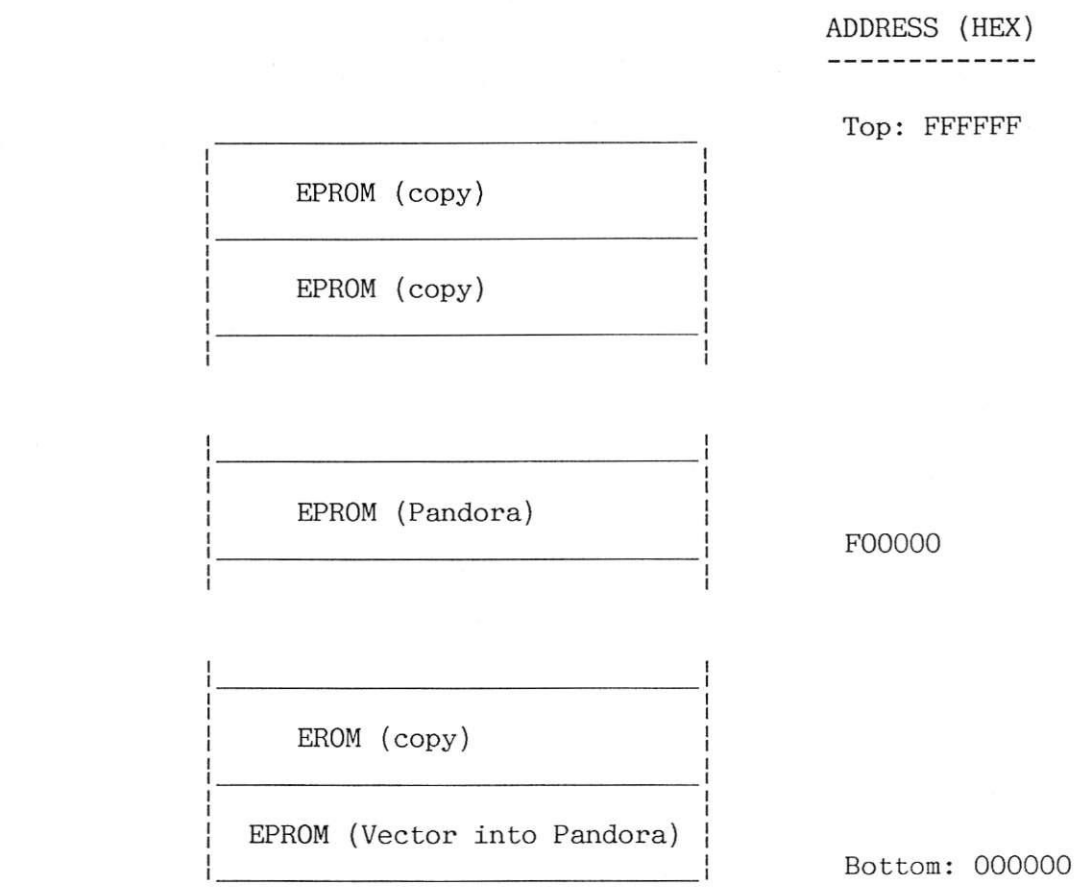
Address map - after Booting

See Fig.3.b

After booting software must address:

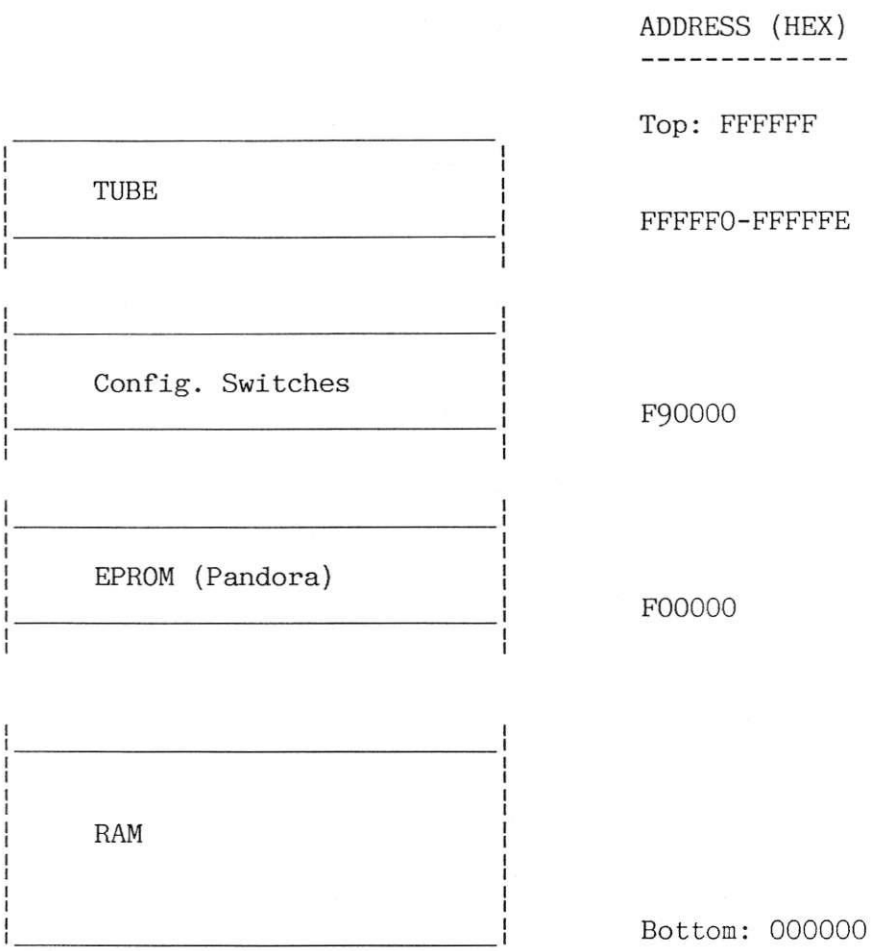
RAM		Hex 000000 to Hex 0FFFFF
EPROM		Hex F00000
Config. Switches		Hex F90000
TUBE	TR1 Status	Hex FFFFF0
	TR1 Data	FFFFF2
	TR2 Status	FFFFF4
	TR2 Data	FFFFF6
	TR3 Status	FFFFF8
	TR3 Data	FFFFFA
	TR4 Status	FFFFFC
	TR4 Data	FFFFFE

FIG.3.a ADDRESS MAP DURING BOOTING



Note: The EPROMs replicate in memory during booting.

FIG.3.b ADDRESS MAP AFTER BOOTING



Note: The address decoding may not be as "tight" as indicated in this diagram.

Address decoding Logic

Multiplexed addresses from the processor or memory manager on AD0-AD15 are latched into IC23 and IC24 and remain stable throught a bus cycle. Address lines A16 to A23 do not require latching as they are not multiplexed.

A23 is used to enable/disable ¦CAS to the memory chips preventing access outside the bottom 4 M bytes (ie when reading other devices).

Address decoding within the 1 M byte is performed by allowing ¦CAS to selected banks only. This is performed by IC28 (address bit A17) according to the following table.

With 64k (256k) bit DRAMs installed:

A17 (A19)	¦CAS Enables
0	Low 1/8th (1/2) M byte
1	Hi 1/8th (1/2) M byte

High Byte Enable (¦HBE) is used together with A0 to enable low and high byte banks according to the following categories (Note: A word located at an ODD address requires two memory cycles).

Category	¦HBE	A0	¦CAS's enabled
Even Byte	1	0	Low byte enabled
Odd Byte	0	1	High byte enabled
Even Word	0	0	Both bytes enabled
Odd Word:			
Odd Byte Followed by Even Byte	0 1	1 0	High byte enabled Low byte enabled

Other categories for Even/Odd Double Word and Quad accesses exist but are simply a repetition of two or more of the above. For more information see NS data sheets for the 32016.

¦RAS plays no part in the address decoding scheme and all RAM devices are RASed on every access. Note this has no effect on the RAMs other than causing the addressed location to be refreshed.

The top 1 M byte is loosely decoded by IC14 to provide chip select signals for the tube (¦TUBE), The configuration links (¦CONFIG), and

the EPROM (¦HPROM). See the previous section on the address map for the correct addresses.

RAS/CAS

One half of the mulitiplexer (IC25/26) is used to supply column addresses to the DRAMs on Latched Address lines LA8-15. Line termination resistors (33 Ohms) are used to reduce reflections on the address lines caused by the high capacitance of the Drams and long length of these tracks. The 9th row and column address bit required by 256k bit DRAMs is provided by IC19 and is A18 during RAS and A17 during CAS.

Refresh

Refresh is performed by inserting wait states into the memory cycle, enabling the refresh address counter (IC27) onto the bus and giving RAS (Known as "RAS only" refresh). IC7 is a binary counter which counts CTTL cycles and generates a refresh cycle every 16uS (approximatly). The RAS timing for this cycle is provided by the sequencer/shift-register based around IC12 and IC13. If a memory cycle is in progress when the refresh access starts it is delayed by ¦CWAIT and restarted when the refresh cycle ends.

Interrupt

The only source of interrupts is the TUBE so there was no need to use an Interrupt Control Unit (ICU NS32202) in this design.

Additional protection against synchronisation failure is provided by latching ¦PIRQ and ¦PNMI on the rising edge of CTTL in IC5 before feeding the interrupts to the processor.

IC6 is a programable device which implements a simple state machine and is used to prevent interrupts from occuring during and just after certain instruction sequences. This device is only necessary when some revisions of the Memory Manager are used and is bypassed by links LK CNM and LK CIR when not fitted.

Memory access cycles

Memory access cycle without MMU

Non memory managed bus cycles are shown in fig.4.a

A memory cycle is initiated by the processor putting an address on the AD bus and pulling ADdress Strobe (¦ADS) low. While ¦ADS is low the address de-multiplexing latch (IC23,24 -LS373) is transparent and the Row address is passed through to the DRAMs. When ¦ADS returns high the address is held in the de-multiplexing latch.

Note: It is not necessary to latch the top eight address bits as they remain valid during the entire bus cycle.

Row address (RAS Cycle)

While ¦RAS is false (HI) the RAS driver bank is enabled and the upper 9 bits are supplied to the DRAMs. In response to ¦ADS going low the TCU after one cycle generates ¦TSO. This in turn causes ¦RAS (DRAM pin 4) to go low and the row address is strobed into the DRAMs.

Column address (CAS Cycle)

¦TSO going low removes the row address from the LA8-15 by making IC24 tristate, and enables the column address via multiplexer IC25 and IC26. ¦TSO low releases the ¦CL -Clear input of IC11 and allows the next CTTL edge to generate ¦CAS and The Column address is strobed into the DRAMs.

Read/write

The direction of the memory access (Read or Write) is signaled to the TCU by Data Direction In (¦DDIN) and it is the TCU that generates READ (¦RD) or WRITE (¦WR) accordingly. ¦WR is distributed to all DRAMs, and ¦RD is used to enable the TUBE and EPROM.

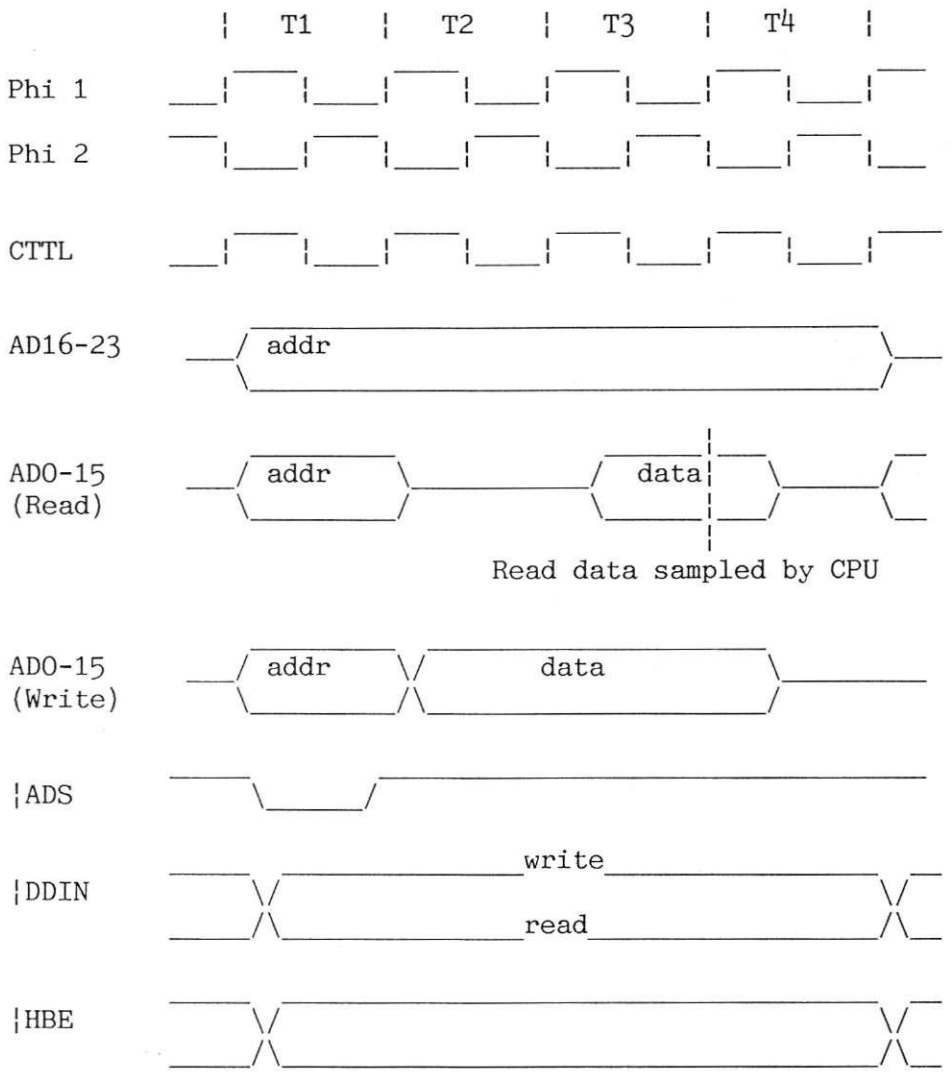
Data validity

During a read cycle the processor expects the data returned from memory to be valid before the end of PHI2 during ¦TS0 low.

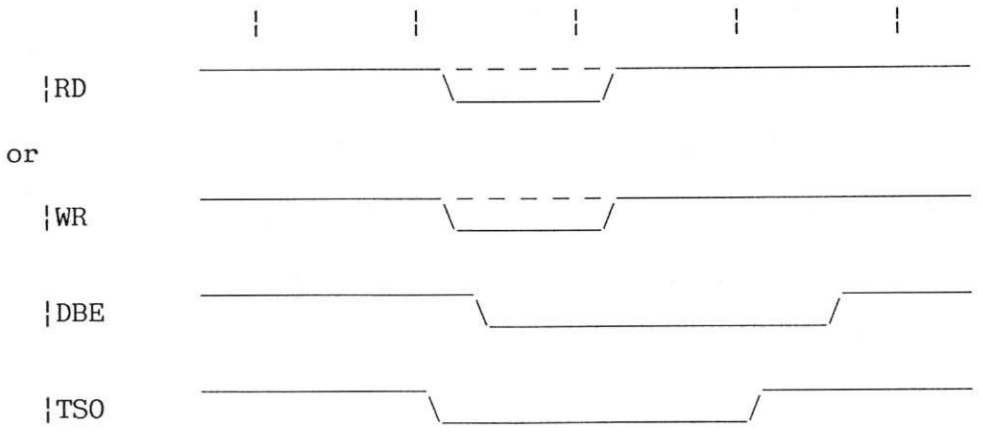
During a write cycle the processor provides valid data during ¦WR low.

FIG.4.a. NON MEMORY MANAGED BUS CYCLE

CPU BUS SIGNALS



TCU BUS SIGNALS



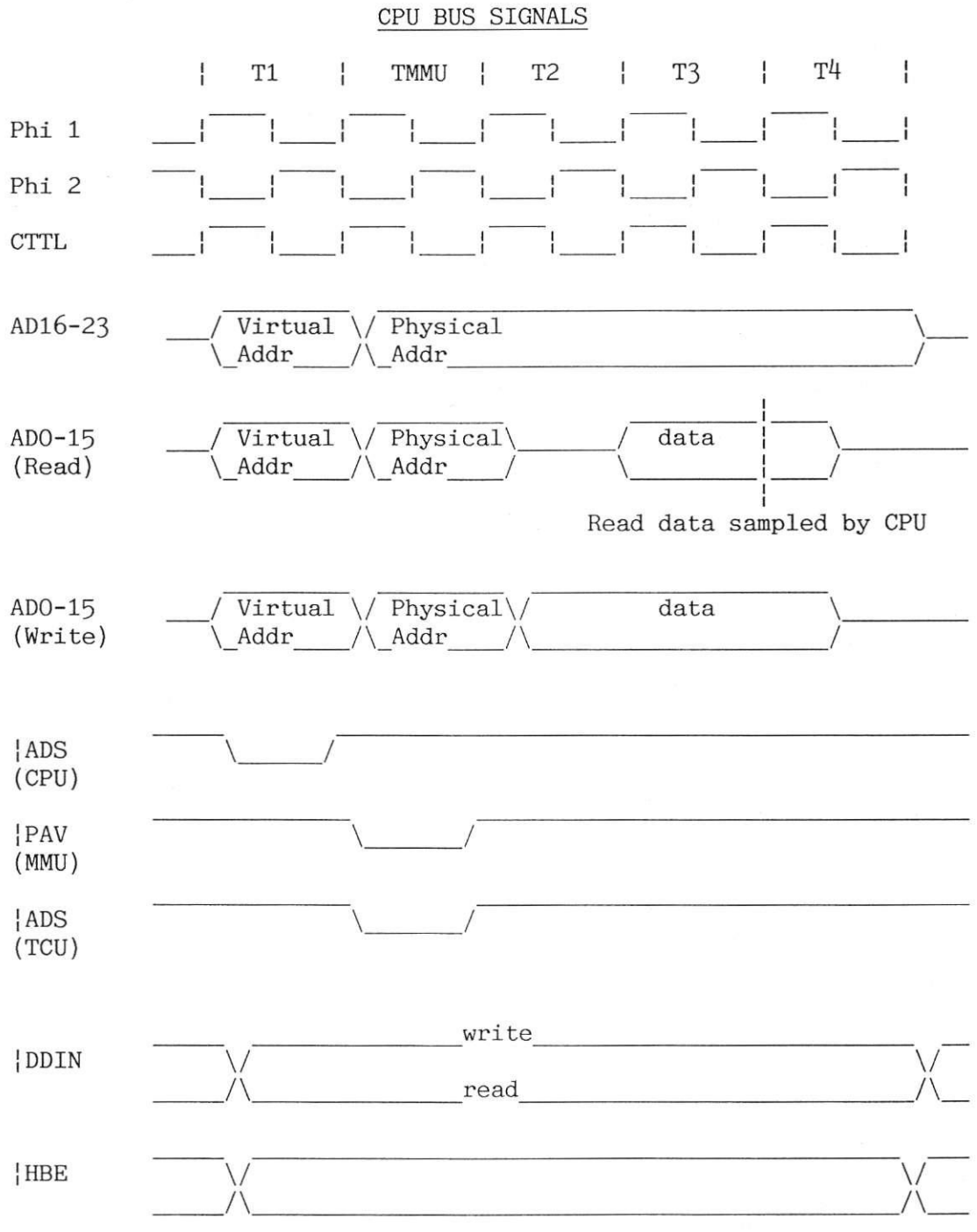
Memory access cycles with MMU.

Memory managed cycles are shown in fig.4.b

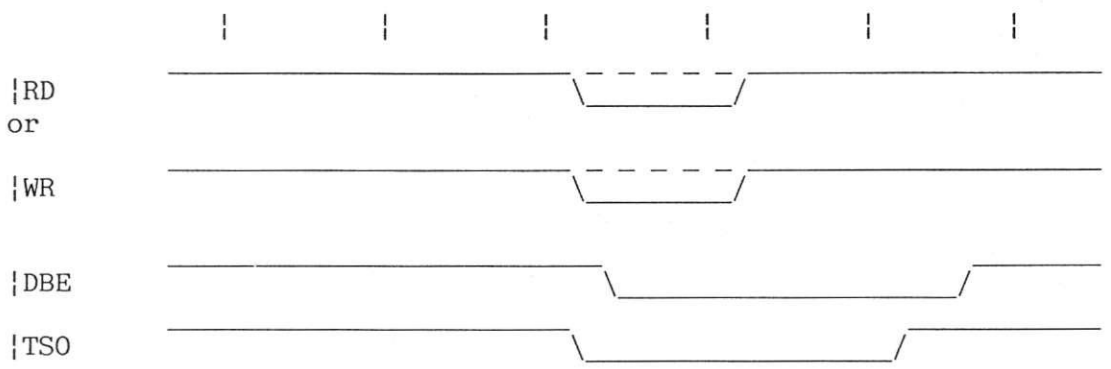
In this case the processor places a VIRTUAL address on the AD bus and ¦ADS from the processor is used to strobe the address into the MMU. The MMU uses an internal translation table to "look-up" the coresponding PHYSICAL address which it places on the AD bus one cycle later. ¦PAV from the MMU looks to the TCU like ¦ADS from the processor and the memory access then continues in the same way as the non-memory managed case but one cycle late.

The memory manager maintains its internal translation table (Cache) without intervention from the processor. If the table entry required is not held in the MMU it is fetched from the larger page table in main memory. In this case the CPU memory cycle is paused while the MMU updates its table entry using a normal memory access cycle. If the MMU detects an illegal access or an access to an address which does not reside in RAM a trap will occur and the trap handling mechanism of the 32016 will be invoked. For a more detailed description of the MMU and its function refer to NS32082 data sheets.

FIG.4.b. MEMORY MANAGED BUS CYCLE



TCU BUS SIGNALS



Links

Configuration

These are read by software on power-up and indicate the presence or absence of optional hardware (ie FPU or MMU). The links have one side connected to OV the other side is pulled high by resistors and can be read onto the AD bus through IC30. A link to OV indicates :

H	No FPU	D	RSVD
G	No MMU	C	RSVD
F	RSVD	B	RSVD
E	RSVD	A	RSVD

Expansion instructions

Memory

The printed circuit board has a total memory capacity of 1 M Byte and can be upgraded to this total by adding using a 512k memory upgrade kit. Acorn Product Code ANB 26.

The memory upgrade kit contains sixteen 256k bit DRAMs which have to be inserted into the empty sockets in the memory array.

IMPORTANT NOTE.

It is strongly advised that DRAMs from different manufacturers are NOT mixed within the same 1 M byte bank. For this reason the upgrade kits will be marked externally with the manufacturers name, and this should be specified when ordering upgrade kits when ever possible.

Memory manager

NYA

Fault Finding

WARNINGS

Before starting it should be realised that any attempt at repair by any person other than a registered dealer or service agent will void the warranty.

Be extremely careful when extracting the 32016 Processor from its socket, it is all too easy to crack the ceramic package and destroy the device which is expensive.

It is assumed that you have available the circuit diagram of the unit, normally distributed with this document.

Equipment Required.

The following is a list of equipment needed to diagnose faults in the 32016 hardware.

(a) U.K. BBC Micro Model B (with disc interface).
(b) An 80 track single disc drive.
(c) Colour/Monochrome monitor.

The minimum test equipment needed in order to trace a fault is a digital multimeter and an oscilloscope. The oscilloscope should have at least two traces and two timebases, and should have a bandwidth of around 50MHz or higher. Other useful pieces of 'test equipment' are: A can of freezer spray; a hair dryer (or commercial hot air blower); a selection of IC test clips (ie Radio Spares 423-627 and 424-018).

Fault Isolation

Unless you have a good idea about where the fault is it is probably best to follow a definite order in testing the unit. To start with there are a number of simple tests which you can use to establish whether the 32016 hardware is working at all.

Visual Check

First perform a visual inspection of the interior of the Coprocessor, check that all external connections (TUBE ribbon cable and the mains lead) are secure and in good condition. Check that no foreign objects (washers etc.) have found their way into the case. Also check that the EPROMs and Molex links are inserted correctly.

Power Supply

Make sure that power is getting to the 32016 board from the on board power supply unit. This means checking for the presence of the +5v supply line and also that the connection to the board is good, the best course of action is to put the DMM across the Faston connectors and check for five volts. You should also check that the PSU is connected to the CPU board the right way round. The tabs are marked OV and +5V so this is just a matter of checking that the red wire is connected to the positive (+5V) tab.

Timing Signals

NOTE: The program found in appendix C will be invaluable as an aid to fault finding when using an oscilloscope.

CLOCKS: Check for the presence of the clock signals XCTL1, PHI1, PHI2 and CTTL (pins 13, 11, 10 and 16 on the TCU). These may be checked against the Fig.2. The TCU generates all system clocks from the double frequency crystal XCTL (FCLK is a buffered version of XCTL). The two clocks PHI1 and PHI2 should have rising edges on alternate rising edges of FCLK. CTTL is just a TTL compatible version of PHI1. Check that these key clock signals arrive at the CPU and FPU where appropriate.

RESET: Check that the system reset is functional by following the sequence of events described in the preceeding text as follows. While alternatly pressing and releasing the break key check for activity on:

HRST - Host Reset - Pin 20, IC1
PRST - Parasite Reset - Pin 37, IC1
RSTI - Reset in (TCU) - Pin 7, IC32
RSTO - Reset out (TCU) - Pin 8, IC32
RSTO - " - Pin 34, IC31
RSTO - " - Pin 15, IC2

All these signals should go low and rise again when the BREAK key is released.

Processor Signals

¦ADS: The lower sixteen lines of the bus are multiplexed address/data lines. The address strobe line, ADS, goes low for approx. a half cycle of PHI1 at the beginning of each bus cycle - indicating a valid address is present on A0-A15. For example when the CPU is executing reads there will be a pulse on ADS (pin 6 of the TCU) approximatly every four clock cycles. The activity on the ADS pin should be checked for as it indicates that the CPU is attempting to access the outside world and is not be completly dead.

¦DDIN: This indicates to the TCU the direction of data on the data bus (ie low indicates data in - read, hi indicates data out - write). Check for activity on this pin. In response to ¦DDIN the TCU generates Read - ¦RD Pin 3, IC4 and Write - ¦WR Pin 4, IC4. Check for activity on these pins.

¦PFS: Program Flow Status. This pin (active low) gives a pulse every time a new instruction begins execution. A stream of pulses on PFS (pin 39) is a good indication that the processor is executing instructions.

¦IRQ: The maskable interrupt line is used whenever information is passed down the tube. It is a bit difficult to get this line active during testing unless you have special test software to run on the 32016 and the machine is in a fit state to run it. Check that ¦INT and ¦NMI are not stuck low.

Boot (start-up) Sequence

The Boot sequence is described in the preceeding text. Having checked that the reset system is operational it is worth examining the signal "BOOTING" which can be found on Pin 6, IC15. This signal is low for a very short period after reset (one or two instructions) and then remains high until the next reset. If this signal is correct it indicates that the processor is able to fetch and execute the first few instructions in the EPROM, and usually the fault is elsewhere.

Tube Signals

After reset the processor should output a message similar to:

PANDORA 32016 version X.XX

Memory size = ... etc

This message is passed through the TUBE by the processor. While this message is being transfered there should be activity on the TUBE chip select Pin 21, IC1. If this message is displayed there is a good chance that the tube is functioning correctly.

Floating Point Faults

If the floating point chip is faulty it will usually show up in one of two ways: It will either not respond when asked to perform floating point arithmetic, or will (more rarely) give the wrong answer.

In the first case the Coprocessor may appear dead because PANDORA checks for the presence of an FPU if the configuration links say there should be one. A quick test would be to remove the FPU configureation link and press BREAK. If the Coprocessor now works the FPU is at Fault.

The second case is difficult to diagnose as the symptoms can appear unrelated to the FPU. The best method of identifying this type of fault it by replacing the suspect FPU with a known good device.

The FPU test supplied with some versions of the Memory test program is very simple and unlikley to detect faults of the second kind.

Memory Faults

Most common faults will be concerned with memory and/or the incorrect instalation of memory upgrade kits. To aid fault finding an EPROM or 80 TRACK DISC based memory test program is available to authorised dealers and production sites (ACORN Product Code ??????). This program is designed to help quickly identify faults in the memory system, and can be used to check that memory upgrades have been installed correctly.

The symptoms of memory failure are varied and include:

(a) Pandora's start-up message incorrectly states the memory size.
(b) Some small programs will run but not other larger ones.
(c) A program will not run with an editor loaded.
(d) Random corruption of files loaded into memory.

The disc based version can be run by inserting the disc in the drive and pressing SHIFT+D while pressing and releasing BREAK. (A !Boot file is provided). The disc version requires some memory itself and so is only useful for testing the memory of an assembled ACW.

The program is also available on two EPROMs which are temporarily inserted in place of the two Pandora EPROMs installed during manufacture. This must be done with the power to the unit switched off or disconnected, and with some care as damage may result from incorrect insertion.

The program writes a fixed pattern into memory and then reads it back checking each word in turn. The pattern written into memory is cycled Hex 21 times because memory faults are often "pattern-sensitive". (This is the main reason that all memory test programs take a long time to run, in this case approximatly 5 mins to test 1 Mbyte. Proportionaly less for smaller machines).

On start-up a menu similar to FIG.5. should be displayed.

You should then press a key between 0 and 7 according to the size of memory installed. Eg. press "2" for 1.5 M byte produces.

```
Select: Testing 1.5 M Bytes

Cycle - XX
```

The "Cycle - XX" message gives an indication of how far the test program has got. The test takes Hex 21 cycles. If a mistake is made in selecting the memory size, then it is quite in order to press BREAK and re-start the program.

Examples of various faults and their corresponding error reports are given in appendix E.

Fig.5 TEST PROGRAM MENU

16032 Test Programs (V2.0)
==========

Key	Test
0	Walking 16 bit memory test (0.5 M bytes)
1	Walking 16 bit memory test (1 M bytes)
2	Walking 16 bit memory test (1.5 M bytes)
3	Walking 16 bit memory test (2 M bytes)
4	Walking 16 bit memory test (2.5 M bytes)
5	Walking 16 bit memory test (3 M bytes)
6	Walking 16 bit memory test (3.5 M bytes)
7	Walking 16 bit memory test (4 M bytes)
8	Refresh test
9	Floating Point Unit (FPU) test

Select:

Appendix A

Circuit Diagram

The circuit diagram has ACORN drawing number 0110,000/C.

Appendix B

Memory Chip/Address Map

Issue 2 printed circuit board:

Address	IC Numbers	
	High byte	Low byte
	D15.....D8	D7.....D0
00000...7FFFF	37 38 39 40 41 42 43 44	29 30 31 32 33 34 35 36
80000...FFFFF	53 54 55 56 57 58 59 60	45 46 47 48 49 50 51 52

Appendix C

Oscilloscope Sync. Aid.

The bus activity during execution of any program (incl. Pandora) will be very random and difficult or impossible to follow with an oscilloscope. The following program when run in the BBC Micro. resets the Coprocessor at a few hundred Hertz. This causes the Coprocessor to repeat the start up sequence rapidly, and provides a triggering mechanisim for an oscilloscope.

The program is written in BBC BASIC.

```
10 ?&FEE0 = &7F
20 REPEAT ?&FEE0 = &A0 : ?&FEE0 = &20 : UNTIL 0
```

This should be entered as follows.

i) Turn off the Coprocessor.

ii) Press BREAK.

iii) Enter the program above exactly as shown.

iv) RUN the program.

v) Turn on the Coprocessor again.

The 32016 is now reseting about 500 times a second. Note that nothing will be displayed on the screen to indicate this.

It is now possible to follow the start up sequence triggering the oscilloscope on the RISING edge of one of the reset signals ie. ¦RST0. First look for this signal on the reset pin of the CPU (pin 34).

It will not be possible to obtain a perfectly stable signal because for various reasons the BBC 6502 does not always execute line 20 in the same amount of time, and the execution of the start-up sequence in the 32016 is disturbed by memory refresh cycles.

Appendix D

Available test software

Title	Media		Code
32016 Memory test/DISC	80 Track Disc		2201,257
32016 Memory test/EPROM	EPROM/ROM	Low	2201,229
		High	2201,230

Appendix E

Test program fault reports

Any faults reported take the following format:

Error addr: HHHHHH - This is the hex address of the fault.

Written: BBBBBBBB BBBBBBBB - This is the binary data written into memory at the faulty address (D15...D8 D7...D0).

Read: BBBBBBBB BBBBBBBB - This is the binary data read back from the faulty address (D15...D8 D7...D0).

Some examples will illustrate how this information can be used to identify a variety of faults. See Fig.6.

Example 1.- A faulty DRAM

In this example bit D5 is "stuck-at-1" but only at a small number of addresses. To find out which DRAM contains this bit at this address use the tables in Appendix B. In this example the fault is in IC52.

Example 2. - Faulty PCB (Data bit) or faulty DRAM

At first glance this looks similar to example one but note that ALL addresses are failing one bit, this could indicate a faulty DRAM, a DRAM in the wrong way around, or a fault on the PCB (ie a short circuit).

Example 3. - Faulty PCB (Address bit)

Because each memory bank has its own set of address buffers a faulty address line may not show up as a fault at all addresses. A typical fault report is shown, note that the pattern read from the memory appears correct but shifted up or down in memory. It is impossible to write a test program that will fully identify faults of this kind which may be caused by an address line shorted to any other signal or power/ground.

Example 4. - Refresh fault

If a random or semi-random pattern is read from the memory, you should suspect a fault in the refresh circuitry. The act of writing or reading refreshes the dynamic memory so this is unlikley to be the cause of a fault reported while testing small amoumts of memory (ie. 1/2 M byte). A refresh test program option is provided.

FIG.E1. MEMORY TEST PROGRAM FAULT EXAMPLES

a/. Faulty DRAM

```
Error addr: 000087B4 Written: 11111111 11111101 Read: 11111111 11111100
Error addr: 00008BB4 Written: 10111111 11111111 Read: 10111111 11111110
Error addr: 000097B4 Written: 00000000 00000001 Read: 00000000 00000000
Error addr: 0000ABB4 Written: 11011111 11111111 Read: 11011111 11111110
Error addr: 0000CBB4 Written: 11101111 11110111 Read: 11101111 11111110
Error addr: 0000D7B4 Written: 11111111 11111111 Read: 11111111 11111110
Error addr: 0000EBB4 Written: 11110111 11111111 Read: 11110111 11111110

                                                    ¦                  ¦

                                                              Stuck bit
```

b/. Faulty PCB (Bit D9) or DRAM

```
Error addr: 00000000 Written: 00000000 00000000 Read: 00000010 00000000
Error addr: 00000002 Written: 10000000 00000000 Read: 10000010 00000000
Error addr: 00000004 Written: 01000000 00000000 Read: 01000010 00000000
Error addr: 00000006 Written: 00100000 00000000 Read: 00100010 00000000
Error addr: 00000008 Written: 00010000 00000000 Read: 00010010 00000000
Error addr: 0000000A Written: 00001000 00000000 Read: 00001010 00000000
Error addr: 0000000C Written: 00000100 00000000 Read: 00000110 00000000
Error addr: 0000000E Written: 00000010 00000000 Read: 00000010 00000000
Error addr: 00000010 Written: 00000001 00000000 Read: 00000011 00000000
Error addr: 00000012 Written: 00000000 10000000 Read: 00000010 10000000
Error addr: 00000014 Written: 00000000 01000000 Read: 00000010 01000000
Error addr: 00000016 Written: 00000000 00100000 Read: 00000010 00100000

                                                              ¦
                                                         Stuck bit
```

c/. Faulty address line

```
Error addr: 00000000 Written: 00000000 10000000 Read: 00000000 00010000
Error addr: 00000002 Written: 00000000 01000000 Read: 00000000 00001000
Error addr: 00000004 Written: 00000000 00100000 Read: 00000000 00000100
Error addr: 00000006 Written: 00000000 00010000 Read: 00000000 00000010
Error addr: 00000008 Written: 00000000 00001000 Read: 00000000 00000000
Error addr: 0000000A Written: 00000000 00000100 Read: 11111111 11111111
Error addr: 0000000C Written: 00000000 00000010 Read: 01111111 11111111
Error addr: 0000000E Written: 00000000 00000001 Read: 10111111 11111111
Error addr: 00000010 Written: 00000000 00000000 Read: 11011111 11111111
Error addr: 00000012 Written: 11111111 11111111 Read: 11101111 11111111
Error addr: 00000014 Written: 01111111 11111111 Read: 11110111 11111111
Error addr: 00000016 Written: 00111111 11111111 Read: 11111011 11111111

      ETC...All even addresses                    Pattern shifted up/down
```

FIG.E1. MEMORY TEST PROGRAM FAULT EXAMPLES (CONT.)

d/. Refresh fault

```
Error addr: 00000002 Written: 01000000 00000000 Read: 00000000 00001000
Error addr: 00000004 Written: 00100000 00000000 Read: 11001001 10010010
Error addr: 00000006 Written: 00010000 00000000 Read: 00101010 01001101
Error addr: 00000008 Written: 00001000 00000000 Read: 00101000 11100010
Error addr: 0000000A Written: 00000100 00000000 Read: 00101010 11001010
Error addr: 0000000C Written: 00000010 00000000 Read: 01011011 01101101
Error addr: 0000000E Written: 00000001 00000000 Read: 10010101 01010010
Error addr: 00000010 Written: 00000000 10000000 Read: 00000100 11011111
Error addr: 00000012 Written: 00000000 01000000 Read: 11000000 00000111
Error addr: 00000014 Written: 00000000 00100000 Read: 10001001 00100101
Error addr: 00000016 Written: 00000000 00010000 Read: 11011011 11100111
```

ETC....All even addresses

Appendix F

Acorn Drawing Numbers

Acorn Cambridge 32016 Co-Processor Specification	0310,000
Acorn Cambridge 32016 Co-Processor Technical Description and Service Manual	0410,000
Acorn Cambridge 32016 Co-Processor Circuit Diagram	0110,000/C

IC No.	0V	5V	TYPE No.
1			TUBE
2	20,25	48	32082
3	20,25	48	32016
4	12	24	32201
5	7	14	74F74
6	8	16	TPB 24S10
7	7	14	74LS393
8	7	14	74LS04
9	7	16	74F08
10	7	16	74S74
11	7	14	74F86
12	7	14	74F114
13	7	16	74LS114
14	7	14	74LS20
15	7	16	74LS00
16	8	16	74LS365
17	7	14	74LS02
18	7	14	74F32
19	7	14	74LS125
20	20,3	24	32081
21	14	28	27128
22	4	28	27128
23	10	20	74LS373
24	10	20	74LS373
25	8	16	S257
26	8	16	S257
27	7	14	74LS393
28	8	16	74LS138
29			
30			
31			4164

ISSUE		F		G		H		J			1		2	
E														
DATE	8-83	8-83		3-84		7-84		14.17.84			AMR857 17.12.84		05/08/85	ECO 30002
DRAWN	BR	BR		MM		BR		MM			MM		PDP	

TOLERANCE	TITLE	©COPYRIGHT 1983 ACORN COMPUTERS Ltd FULBOURN ROAD CHERRY HINTON CAMBRIDGE CB1 4JN
FINISH	32016 2nd PROCESSOR CIRCUIT DIAGRAM (4 LAYER PCB)	
MATERIAL	DRG. No. A00110,000/C	ACORN COMPUTERS Ltd