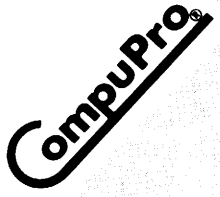

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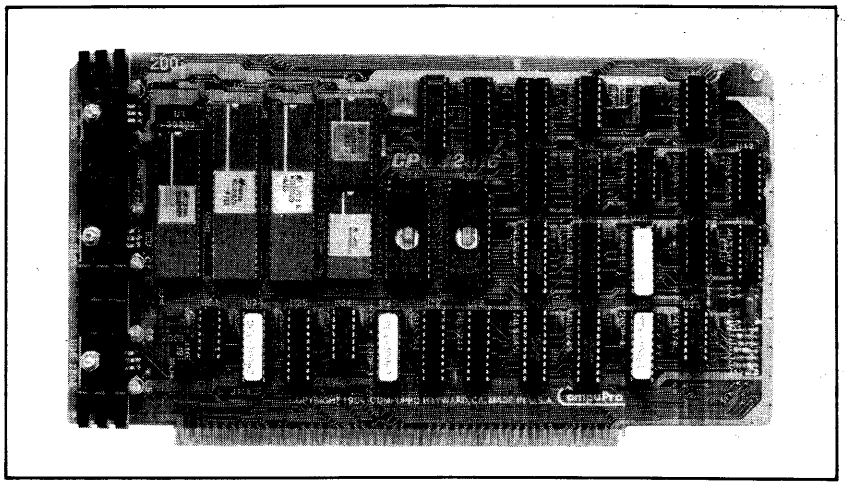
CPU 32016

Technical Manual



HIGH PERFORMANCE 32-BIT NS32016
WITH
NS32081 IEEE FLOATING POINT PROCESSOR
NS32082 MEMORY MANAGEMENT UNIT
NS32202 INTERRUPT CONTROLLER
EPROM SOCKETS FOR UP TO 32K

CPU 32016 TECHNICAL MANUAL

Hayward, CA 94545

First Edition: October,1984

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Board No: 200 Revision: B

CONTENTS

HOW TO GET YOUR CPU 32016 UP AND RUNNING WITHOUT READING THE MANUAL

This section is for those of you who are running this CPU board in a standard CompuPro configuration and do not intend to deviate from that standard configuration. You should be able to set jumpers as shown below and never have to change them again (unless you change your system configuration).

If you want to know all the details about what these jumpers do, you will have to read the rest of this manual.

CPU 32016 INSTALLATION PROCEDURES

STEP 1. UNPACK CPU 32016 BOARD.

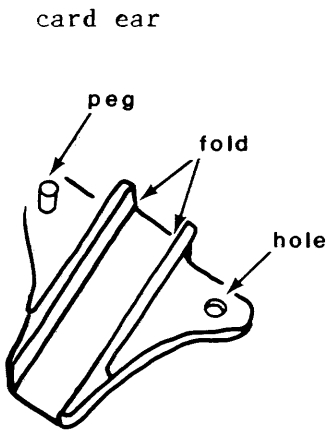
Along with the board, you will find two card ears in the plastic bag.

STEP 2. INSTALL CARD EARS.

a) Hold the board so the component side is toward you.

b) Insert the peg on the card ear into the hole in the right corner of the board. Fold the ear over the board's edge until the ear's hole snaps over the peg (make sure the long edge of the ear is along the top edge of the board.

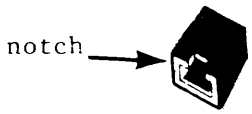
c) Repeat for left ear.



STEP 3. INSTALL JUMPER SHUNT CONNECTORS

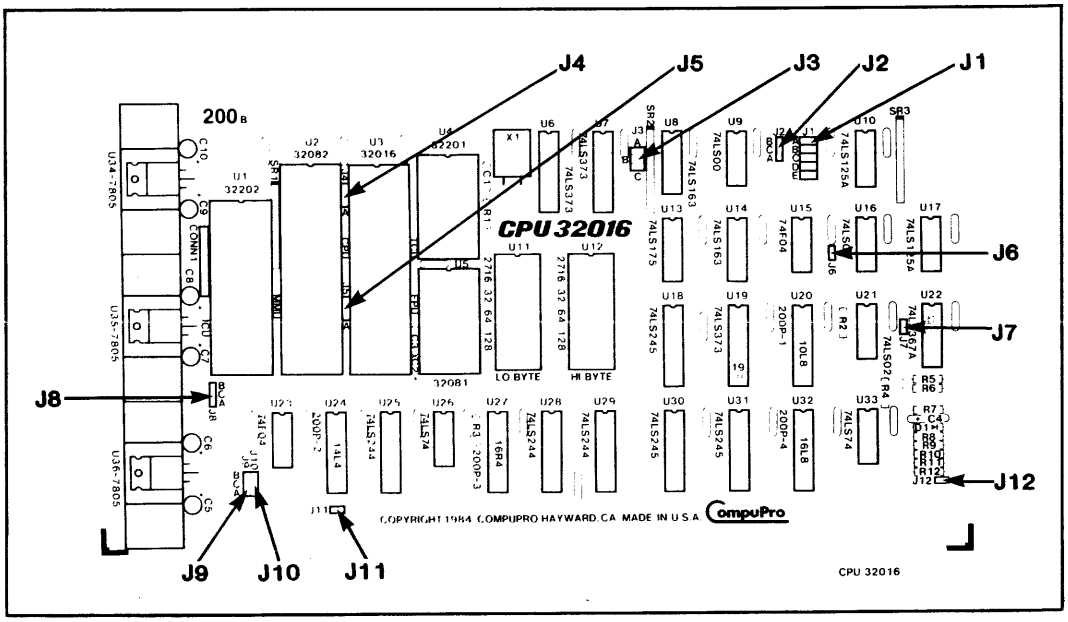
Make sure the jumper shunts are installed as listed below. (See figure 1 for the location of jumper connectors J1 through J12.

JUMPER SHUNTS

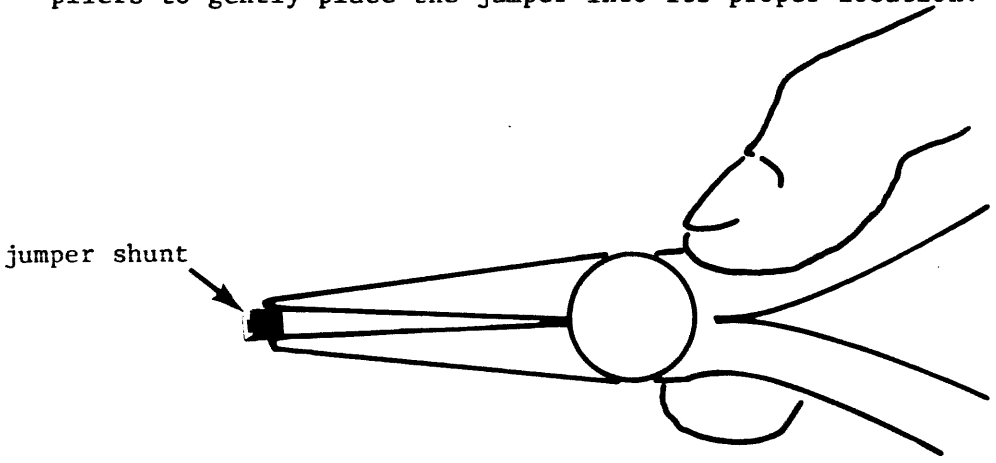


A jumper shunt is a small plastic part used to connect two pins on the jumper connector. Jumper shunts should be installed notch side up.

Figure 1. CPU 32016 Jumper Location



To jumper the board correctly, use a pair of needle nose pliers to gently place the jumper into its proper location.



J1 should be connected across position C.

J2 should not be installed.

J3 should be connected:
for a 6MHz CPU, across positions B and A;
for an 8MHz CPU, across position C;
for a 10MHz CPU, across positions C and A:
for a 12MHz CPU, across positions C and B.

J4 should be connected:
with MMU installed, across bottom two pins A-C;
without MMU installed, across top two pins B-C.

J5 should be connected:
with MMU installed, across top two pins B-C;
without MMU installed, across bottom two pins A-C.

J6 should not be installed.

J7 should not be installed.

J8 should be connected:
with MMU installed, across top two pins B-C;
without MMU installed, across bottom two pins A-C.

J9 should not be installed.

J10 should not be installed.

J11 should not be installed.

J12 should not be installed.

NOTE: SWITCH SETTINGS FOR OTHER COMPUPRO BOARDS

Follow the switch settings as outlined in the Disk 1A manual for the CPU 32016.

BOOTING UP THE SYSTEM

If all the switches and jumpers in the system are set correctly (make sure your drives are jumpered per the Disk 1A manual if they are other than CompuPro drives), you should be ready to boot up the system. Make sure that all the boards are plugged squarely into the motherboard, replace the enclosure's cover, and turn on the power to the computer, terminal and disk drives. The light on your "A" drive should be flashing about once per second. If it is not flashing, stop! Read the Disk 1A manual's troubleshooting section and correct the problem before proceeding. If the light is flashing, insert the boot diskette into the A drive and close the drive door. Your system should sign on.

ABOUT THE CPU 32016

The CPU 32016 from CompuPro is one of the most advanced processors available for the IEEE 696/S-100 Bus. Based on National Semiconductor's high performance NS32016 32-bit microprocessor, it includes sockets for the NS32082 Memory Management Unit, the NS32081 IEEE Floating Point Unit, the NS32202 Interrupt Control Unit, and up to 32K of onboard EPROM.

Powerful features of CPU 32016 include:

* A symmetrical instruction set specifically designed to support high level languages such as C, Pascal, or Ada

* Nine vectored hardware interrupts, eight vectored software interrupts, and two fully programmable timers

* Optional demand paged virtual memory management with dynamic address translation, memory protection, and extensive debugging support facilities

* Optional single and double precision IEEE floating point operations using all addressing modes of the processor

The CPU 32016 also includes circuitry that allows it to handle 8- and 16-bit memory and I/O devices that conform to the IEEE 696/S-100 protocol for 8- and 16-bit transfers. Both 8- and 16-bit types may be mixed in a system; the CPU 32016 will dynamically adjust itself to the proper bus width. The CPU 32016 is fully compatible with DMA devices that adhere to the IEEE 696/S-100 standard protocols (like the DISK 1A, DISK 2, DISK 3, MPX-1 etc.).

The CPU 32016 currently operates with a 6 MHz clock, but was designed and tested at higher speeds and will accommodate faster parts when they become available. A flexible internal wait state generator facilitates the use of slow I/O or memory in faster systems.

A special clock switching circuit allows the use of specially designed slave processors to share the bus with the CPU 32016. Devices using this special clock switching feature are free of the CPU clock and are able to execute bus cycles either faster (in the case of a high speed DMA channel) or slower (in the case of a slow peripheral) than the CPU clock.

Couple high speed 32-bit operation with powerful IEEE 696/S-100 features and you get the CPU 32016, truly a processor board for the advanced computing systems of the eighties. Congratulations on choosing a CompuPro product.

JUMPER SELECTION

This section will provide a detailed description of all the jumper settings for the CPU 32016. To set the board up for use in a standard CompuPro system configuration, see the first section of this manual: "How to Get Your CPU 32016 Up and Running Without Reading the Manual".

Jumpers J1 and J3 are multi-pin jumpers at which shunts should be placed horizontally at the proper location(s). Jumpers J2, J4, J5, J8, J9, and J10 are three pin jumpers at which shunts should be placed vertically on the top two pins (B-C), on the bottom two pins (A-C), or removed entirely. Jumpers J6, J7, J11, and J12 are two pin jumpers where shunts should either be installed or removed.

J	Position	Function
1	A	2 I/O WAIT STATES
	B	2 MEMORY WAIT STATES
	C	1 I/O WAIT STATE
	D	1 MEMORY WAIT STATE
	E	1 WAIT STATE FOR ALL CYCLES
2		A-C FOR S-100 NMI; B-C FOR MMU NMI
3	A	FOR 6,10 MHz
	B	FOR 6,12 MHz
	C	FOR 8,10, AND 12 MHz
4		A-C FOR MMU; B-C FOR NO MMU (PAV/ADS)
5		A-C FOR NO MMU; B-C FOR MMU (HLDA/HLDAO)
6		EPROM BOOT (POWER ON JUMP)
7		MWRT GENERATION BY CPU 32016
8		A-C FOR NO MMU; B-C FOR MMU (RSTO/ABT)
9		B-C FOR 27128; A-C FOR OTHERS
10		B-C FOR 2716; A-C FOR OTHERS
11		MMU A24 TO S-100
12		ϕDSB* ENABLE

Jumper J1 - This jumper controls the number of internally generated wait states that are inserted in a particular type of operation. As all 32016 operations are memory mapped, this jumper

simply controls which sections of memory receive internally generated wait states. The sections of memory referred to as **I/O+** are page FEh (I/O), page FFh (Internal EPROM and ICU), and locations 0h through 7FFh (low memory). The sections of memory referred to as **MEM** comprise the rest (800h through FDFFFFh). Where the shunts are placed controls how many wait states are inserted into **MEM** or **I/O+** cycles. Position A and B should never be installed simultaneously, and, similarly, positions C, D, and E should never have more than one shunt. Wait states are additive, i.e., installing positions C and A puts three wait states in I/O+ cycles. Installing no shunts introduces no wait states. J1 is located between U9 and U10.

I/O+	-	0 to 7FFh, FE0000h to FFFFFFh
MEM	-	800h to FDFFFFh

Position	E	-	Inserts one wait in every cycle
	D	-	Inserts one wait in **MEM** cycles
	C	-	Inserts one wait in **I/O+** cycles
	B	-	Inserts two waits in **MEM** cycles
	A	-	Inserts two waits in **I/O+** cycles

Jumper J2 - This jumper controls whether the 32016 NMI input (non-maskable interrupt) comes from the S-100 NMI* or the MMU interrupt output. It is normally connected on the solder side of the PC board to the S-100 NMI*. Pins for this jumper are not normally installed. If it should ever be necessary to have the MMU interrupt output assert NMI (as is suggested by National for some diagnostic modes), cut the trace connecting A-C of the jumper, install pins, and place the shunt in the top (B-C) position. J2 is located between U9 and U10 to the left of J1.

Position	A-C	-	S-100 NMI* goes to 32016 NMI
	B-C	-	MMU interrupt goes to 32016 NMI

Jumper J3 - This jumper is used to control what the CPU clock frequency is divided by to produce the 2 MHz S-100 CLOCK signal. Positions to produce the required 2 MHz for various CPU speeds are given. No other CPU speeds are acceptable if this signal is to be produced properly. J3 is located between U7 and U8.

2MHz; position A
4MHz; position B
6MHz; positions B and A
8MHz; position C
10MHz; positions C and A
12MHz; positions C and B
14MHz; positions C and B and A

Jumper J4 - This jumper controls what signal latches addresses and initiates an S-100 bus cycle. In systems without the 32082 MMU, ADS (address strobe) from the 32016 CPU latches addresses from the multiplexed Address/Data bus. In systems with the MMU, PAV (physical address valid) latches the addresses. J4 is between U2 and U3, near pin 4 of U3.

Position	A-C	-	MMU installed
	B-C	-	MMU removed

Jumper J5 - This jumper controls whether S-100 HLDA* is generated by the MMU or CPU. When the MMU is installed, HLDA* must be generated by it. J5 is located between U2 and U3, near pin 17 of U3.

Position	A-C	-	MMU removed
	B-C	-	MMU installed

Jumper J6 - The CPU starts executing after reset at location 0h. The BOOT feature allows the onboard EPROM to appear at this low memory long enough for the CPU to execute a jump into the normal EPROM location at FF0000h.

This jumper determines whether the on board EPROM is forced on immediately following a system reset (POC* or RESET*). When installed, after reset the CPU will start executing in the EPROM and continue executing in the EPROM until the first processor write cycle at which time the EPROM will revert to its normal spot at 00FF0000h. During this BOOT time, the EPROM appears in all of memory. The first write should be a word write. An easy power-on-jump can then be made by placing the following code at the start of the EPROM:

```
BOOT:   LPRD SP,00FF0020h       ;sp in EPROM
        JSR  @START             ;start of code
```

Location START is often in the EPROM (i.e. 00FF0010h) so that the jump to subroutine both disables the EPROM in low memory and jumps to the EPROM's normal location to start executing. When this shunt is removed, BOOT is never asserted, the CPU starts executing at location 0h on the bus, and the EPROM only appears at 00FF0000h. J6 is located between U15 and U16.

Inserted	-	EPROM enabled on BOOT
Removed	-	EPROM only appears in high memory

Jumper J7 - This jumper controls whether MWRT is asserted by the CPU 32016 or by the front panel in older IMSAI systems. It is a normally closed connection that allows the CPU 32016 to drive the MWRT signal onto the S-100 bus pin 68. In older IMSAI type systems, MWRT was often generated by the front panel and needed to be disconnected on the CPU. If it is ever necessary to use this feature to disable MWRT, the trace under J8 can be cut and pins installed to reconnect it when necessary. Pin 3 on buffer U22 can also be removed from the socket to achieve the same result. Systems with all CompuPro boards will never need this modification and should leave J7 not installed. J7 is located between U21 and U22.

Inserted	-	MWRT generated by CPU 32016
Removed	-	MWRT not generated by CPU 32016

Jumper J8 - The MMU uses a short pulse on the RESET input to the CPU to indicate a bus cycle must be aborted due to a page fault or other error. Thus, when the MMU is installed, it generates the 32016 RESET and the shunt must be across B-C. When there is no MMU present, RESET from the 32201 goes directly to the 32016 and the shunt must be across A-C. J8 is located below U1, near pin 20.

Position	A-C	-	MMU removed
	B-C	-	MMU installed

Jumpers J9 and J10 - These two jumpers select the proper address lines to go to the onboard EPROM sockets. Regardless of these settings, the EPROM will always appear from memory location 00FF0000h to 00FF7FFFh, with EPROMs smaller than 27128s duplicating themselves through the whole space. J9 and J10 are located to the left of U23.

Size	2Kx16	4Kx16	8Kx16	16Kx16
EPROMs used (2)	2716	2732	2764	27128
J9 position	A-C	A-C	A-C	B-C
J10 position	B-C	A-C	A-C	A-C

Jumper J11 - Due to its virtual memory capabilities, the MMU is able to generate 25 lines of address. If it is desired to bring the 25th address line (A24) out to bus NDEF pin 65, the necessary pins and shunt can be inserted in J12. Notice that the current drive on this line does not satisfy IEEE 696/S-100 drive requirements. National suggests that this line can be used when doing emulations. J11 is located below U25.

Jumper J12 - This shunt inserted allows the master bus clock (ϕ) to be disabled by a temporary bus master asserting the ϕDSB* signal on bus line 21. When the shunt is removed, this feature is disabled. This new S-100 bus line has been defined by CompuPro for use with our possible future slave processor boards or special DMA peripherals. For now, leave this shunt removed. The manual supplied with a board that utilizes this line will instruct you to install the shunt. For a description of how the ϕDSB* line is implemented, see the Theory Of Operation section of this manual. J12 is located to the right of U33, below R11.

This completes the section on jumper selection.

INSTALLING THE MEMORY MANAGEMENT UNIT or FLOATING POINT UNIT

The CPU 32016 has been designed to accept both the NS32082 MMU and/or the NS32081 FPU. Both sockets have been fully tested at the factory and are ready to accept devices rated at the speed of the processor.

If you are not familiar with this hardware or have never inserted a large IC into a socket, the time to learn is not with a several hundred dollar part; it is too easy to break a pin and ruin the IC. A factory upgrade includes parts (the MMU and/or FPU) and a complete confidence test. Contact your CompuPro account representative for current upgrade information.

If you chose to install the FPU or the MMU yourself, follow these instructions carefully. For the FPU, simply plug the device into the socket labeled U5. For the MMU, plug the device into the socket labeled U2, move jumper J4 from B-C to A-C (top to bottom pair), move jumper J5 from A-C to B-C (bottom to top pair), and move jumper J8 from A-C to B-C (bottom to top pair). The software can then execute the SETCFG instruction to enable the instruction sets of the associated slaves.

THEORY OF OPERATION

This section of the manual will explain, in general, how the circuitry on the CPU 32016 works. In the following discussion, it will be helpful to refer to the schematic diagrams contained in the appendix of this manual.

The CPU 32016 is based on the National Semiconductor NS32016. Non-overlapping clocks (ϕ1 and ϕ2) for the CPU and MMU are generated by the 16201 clock generator IC (U4). It uses an external crystal (X1), a series resistor (R1), and a capacitor (C1). The crystal is a fundamental (parallel) type, and is twice the desired processor frequency.

In addition to the two clocks used by the CPU and MMU, the 16201 generates CTTL and FCLK. CTTL is a processor speed clock used to generate timing for the S-100 bus, and FCLK is a crystal speed clock used to generate the 2 MHz clock and the proper width for pSTVAL*. CTTL synchronizes interrupt inputs and generates strobes (pWR* and pDBIN) during byte serialized transfers. CTTL* is buffered through U17 pins 11 and 12 to give the S-100 bus ϕ, which is in turn used to run the finite state machine (PAL U27/200p-3) that gives pSYNC as well as the signals needed by the byte serializer (ASSERT-A0*, TWO-CYCLE*, and USTBINH*). The tri-state enable (pin 13) of the bus ϕ buffer is driven by the inverting output of flip flop U33b. The D and CLR inputs to this flip-flop are driven by the CompuPro defined bus line ϕDSB* on pin 21 of the S-100 bus. This line will be driven low by a temporary master coincident with the CDSB* signal (which is just after the rising edge of the clock). This will immediately cause the bus clock to be tri-stated. Pull-up SR3 makes sure that it floats to the high state, but the temporary master should be driving the clock now anyway. When the temporary master relinquishes the bus, it will drive CDSB* high and float its clock high. Flip-flop U33b will then be free to enable the CPU 32016's clock, but not until after the next rising edge of it. This ensures that there are no slices on the clock line.

The 32016 (U3) has two tightly coupled slaves: the Memory Management Unit (U2) and Floating Point Unit (U5). They communicate over the data bus and other lines, and use the SPC signal to coordinate two clock cycle data and command transfers. The FPU can be inserted into a system and have its instruction set and registers (F0-F7) declared operational simply by using the SET CONFIGURATION instruction. The MMU requires the SET CONFIGURATION command in addition to changing the positions of three jumpers (J4, J5, and J8). The MMU informs the CPU that it is in the system and will be doing address translation (even if the physical address is the same as the virtual address) by driving the SPC line low during RESET. On the rising edge of RST0*, the CPU samples SPC and if it is low, alters its basic bus state sequence to conform to the MMU's requirements. The most obvious difference is the change of bus state sequence from T1,T2,T3,T4 to T1,Tmmu,T2,T3,T4. Address translation requires one extra clock cycle in every bus cycle. T1 was initially used to transfer the physical address from the CPU to

the bus but is now used to transfer the virtual address to the MMU. Tmmu now is used by the MMU to transfer the physical address to the bus. The MMU produces 25 address bits for a total addressable range of 32 Mbytes. Although address bit A24 is not defined on the S-100 bus, the CPU 32016 provides a jumper for this line to S-100 NDEF line 65. The low output current drive of the MMU does not meet S-100 driver specs. Actual measurement of this output show that it will easily supply several LS inputs from the bus. National considers this bit ideal for trapping back and forth between partitions of memory when doing in system software debugging.

The 32016 communicates with the 32202 Interrupt Control Unit through 64 addresses: FFFE00h to FFFE3Fh. These addresses are decoded to ICUCS* (PAL U24). ICUCS* is actually decoded from FFF800h to FFFFFFh so the ICU appears many times through the 2K range. This is only a problem when using NMI* as the NMI* acknowledge cycle will appear as an INTAK cycle to the 32202. It is sufficient to re-initialize the 32202 after every NMI*. The ICU interrupt output generates INT* on the S-100 bus, and is sychronized by U13 for the 32016. The 32202 is implemented in the 8 bit bus mode, so only the low eight bits of data are used. G0/IR0 through G7/IR14 are brought to CONN 1. For information on these lines, see the National 32202 data sheet. The two internal 16 bit counters are clocked with the 2MHz clock. The NMI* bus pin 12 is synchronized by U13 for the 32016. It must be held for at least 1 clock cycle to guarantee service. In some diagnostic modes, MMUINT* might need to be tied to the non-maskable input of the 32016 (J2).

An S-100 bus cycle is initiated by START* which is asserted on LATCH* (either ADS or PAV), and cleared on the next rising edge of CTTL (U26a). The trailing edge of LATCH latches the address off of AD0-AD15 into the two 74LS373s (U6 and U7). The address lines are buffered by U25, U28, and U29 to the S-100 bus. Shortly after the start of a cycle, the CPU 32016 must choose between two possibilities: a one-cycle or a two-cycle fetch. A one-cycle fetch is when the processor requests either 8 or 16 bits from a slave and the slave is able to handle the transfer in one S-100 bus cycle. A two-cycle fetch is when the processor requests 16 bits from a slave but the slave is only able to transfer 8 bits, forcing the internal finite state machine to complete two S-100 bus cycles to fetch two bytes before allowing the 32016 to complete its cycle. A two-cycle fetch is also called a byte serial fetch. The decision to execute either a one-cycle transfer or two-cycle transfer is controlled by the S-100 signals sXTRQ* and SIXTN*.

The sXTRQ* line is generated in PAL U32 from HBE* and LA0. If HBE* and LA0 are low, sXTRQ* is asserted. If the addressed slave board asserts SIXTN* indicating that a 16-bit transfer can occur, the CPU completes the transfer at full speed. An S-100 cycle starts with pSYNC being asserted on the rising edge of bus ϕ when START* is asserted. pSYNC lasts for exactly one cycle and is synchronous with CTTL*. pSTVAL* falls on the next low level of FCLK following pSYNC rising (U26b). The strobes pDBIN and pWR* are generated with DDIN* and TSO* and are synchronous with CTTL. In a bus cycle with no wait states, pDBIN is asserted for 2 complete clock cycles, and pWR* for

one and one half. When internal wait states are used, the 74LS125 (U10) generates W1 or W2 into the counter (U14). At the end of START*, C0 goes low and generates CWAIT* to the 32201 through U27. When the counter finishes (reaches 15), C0 goes back high and the cycle ends. External wait states are generated by RDY*. Note that XRDY* is not accepted by the CPU 32016. This is not a problem in CompuPro systems as no CompuPro boards assert this signal.

When no slave asserts SIXTN*, SET-TWO* is asserted to indicate that a byte serialized transfer is necessary. On the rising edge of bus ϕ at the trailing edge of pSYNC, U27 generates TWO-CYCLE*. As soon as U27 recognizes that a byte serialized transfer is necessary, the 32016 is put in a wait state by CWAIT* to give the state machine time to make two S-100 bus cycles. With no other wait states, a total of 7 (instead of 4) clock cycles are needed to get the data. When neither RDY* nor C0 are asserted requesting wait states during the first bus cycle, USTBINH* is asserted. Two CTTL clocks later (through U13), STBINH* causes the strobes to go unasserted for one clock cycle synchronous to CTTL. ASSERT-A0 and pSYNC are asserted on the next rising edge of CTTL* after the strobe falls. The second cycle finishes when the 32201 finishes its wait states and RDY* is not asserted. Internal wait states are controlled during the first S-100 bus cycle by counter U14, and by the W1 and W2 inputs to the 32201 during the second bus cycle.

The data bus is buffered, multiplexed and latched (depending on what is required) by U18, 19, 30, and 31. The control of these buffers and latches is performed by a 10L8 PAL 200P-1 (U20). DDIN* determines the direction of data (read or write) and goes to the direction inputs of the the main data bus buffers (U18 and U31). The signal DBE* coming from the 32201 determines when data can be put on the CPU 32016's internal bus or the S-100's data bus. The rest of the inputs to the PAL control which of the various buffers are enabled. The LA0 and DDIN* signals control the basic 16 bit cycles, while ASSERT-A0 and pDBIN signals control the buffers during a byte serial transfer. At the trailing edge of the first pDBIN in a byte serialized read, the low data is latched off the DI bus by U19. The address is incremented for the second cycle by ASSERT-A0, and a second strobe is generated. The data is read by the 32016 through U31 and from U19 toward the end of the second pDBIN. A write cycle is similar except data is passed through U18 to the DO bus for the first pWR*, then passed through U30 for the second pWR*.

The S-100 status lines are generated by a 16L8 PAL 200P-4. As the ST1-ST3 lines can change immediately at the beginning of T4, S-100 status lines are latched in the PAL by the signal START*. SDSB* tri-states all of the outputs. The statuses are arranged as such:

Signal	ST3-ST1	DDIN*	I/O*
sHLTA	000	x	x
sINTA	010	0	1
sM1	100	0	1
sMEMR	1xx	0	1
sINP	101	0	0
sOUT	101	1	0
sWO*	101	1	x

The on-board EPROM sockets (U11 and U12) are decoded by PAL U24 (200P-2). PROMSEL* is asserted from memory addresses FF0000h to FF7FFFh, a 32K window. While PROMSEL* is asserted, the external S-100 buffers (U18, U19, U30, U31) are not enabled. Jumpers J9 and J10 choose the proper pinout for the devices. 2716s require Vcc to pin 23 of the socket, and 27128s require LA14 to pin 26 of the socket. Note that WR* can be brought to pin 23 of the socket by J11 so 6116 type RAMs can be used. It is not possible to make byte writes to the sockets, though, so care should be taken to make only word or double word writes on even boundaries to the on board RAMs.

PAL U24 divides memory up into the ICU space (FFF800h to FFFFFFh), PROM space (FF0000h to FF7FFFh and BOOT*), I/O space (FE0000h to FFEFFFh), and the rest (memory space). The final output of the PAL is I/O+* which controls the internal wait state generator. The wait state selector (J1 with U10) is set up so that a given number of wait states are inserted when I/O+* is asserted, and a different number is inserted when I/O+* is not asserted. In the factory PAL, I/O+* is asserted from FE0000h to FFFFFFh (I/O, ICU, and PROM), and from 0h to 7FFh (often an external BOOT EPROM). Under the CompuPro suggested jumper setting, this would mean that fast system memory (800h to FDFFFFh) would receive no wait states, where the other sections (I/O, PROM, ICU, and low memory) would receive 1. Of course, a new PAL could be burned with an appropriate PAL programmmer to place I/O+*, PROMSEL*, or I/O* anywhere in the 16 Megabyte memory map.

Jumper J3 controls the divider to generate the 2MHz clock. LOAD is asserted to the 74LS163 whenever the output is 6. The next FCLK loads a new value (0 thru 7), toggles 2MCLK, and restarts the counter. By choosing the right value to load, any CPU speed between 2MHz and 14MHz can generate the 2MCLK. Make sure that this 2MHz is indeed being generated because the ICU requires the 2MHz clock for its counters.

The power fail circuit (U33) causes a POC* to be issued upon the rising edge of PWRFAIL*. This insures that the system will recover just as if the power had come on for the first time, and prevents problems that might occur if the power dips for a short period causing PWRFAIL* to be asserted, but the power doesn't actually go away.

Typical S-100 bus timing specifications for the CPU 32016 board are given below. They are representative of a typical board only, and are not intended to present either minimum or maximum ratings.

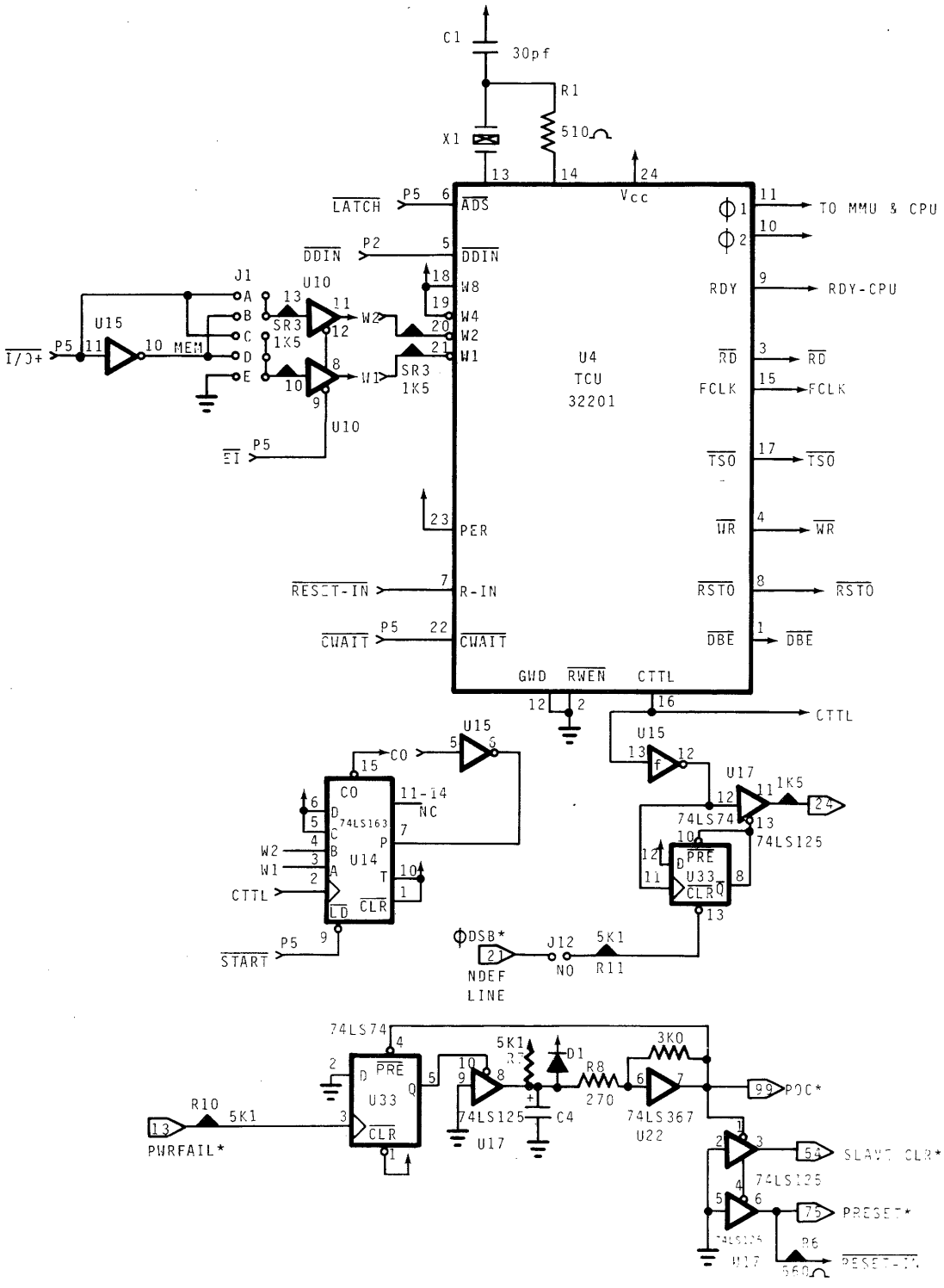
Definitions of the nomenclature is given in the IEEE Std 696-1983, obtainable from the Institute of Electronic and Electrical Engineers. All specifications are in nano-seconds and are for a board running at 6 MHz.

Specification		Typical Value	Description
tCY		166	Clock cycle time.
tCYH		88	Clock high time.
tCYL		72	Clock low time.
tϕSY		13	From bus ϕ to pSYNC.
tSY		156	pSYNC width.
tST*ϕ		115	pSTVAL to bus ϕ.
tST		515	pSTVAL high.
tST*		150	pSTVAL low.
tAST*	A0	70	Address set up
	A1-A15	90	prior to pSTVAL.
	A16-A23	110	
tSST*		80	Status set before pSTVAL.
tDB		350	pDBIN width.
tST*DB		60	pSTVAL to pDBIN.
tDB*SY	8 Bit	80	End pDBIN to pSYNC.
	16 Bit	240	
tDB*AS		160	Address, Status hold.
tACC		305	pSTVAL to data req'd.
tWR*		250	pWR* width.
tST*WR*		135	pSTVAL to pWR*.
tWRSY	8 Bit	80	End pWR* to pSYNC.
	16 Bit	240	
tDWR*		70	DO valid to pWR*.
tWRASD		160	Address, Status, DO hold.
tWR*MR		23	pWR* to MWRT.
tRDYϕ	RDY	20	Calculated minimum set up
	SIXTN	30	time accepted by CPU.
tϕRDY		10	Calculated hold req'd.
tSYST*		34	pSYNC to pSTVAL.
tAϕ		180	Address to ϕ.
tST*ϕ		200	Status to ϕ

This completes the Theory of Operation section of this manual.

LOGIC DIAGRAM

1 of 6



CPU 32016
200B
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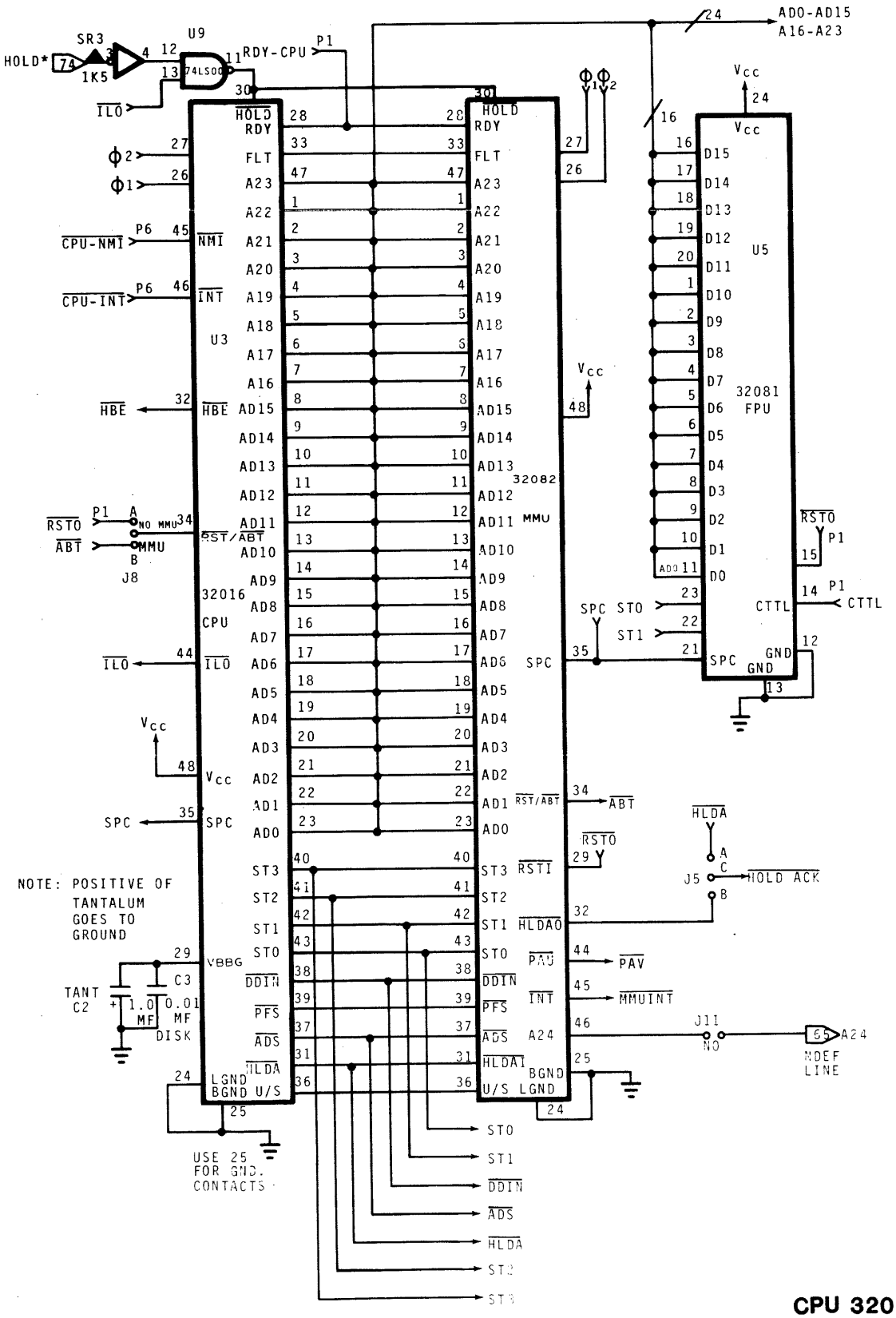

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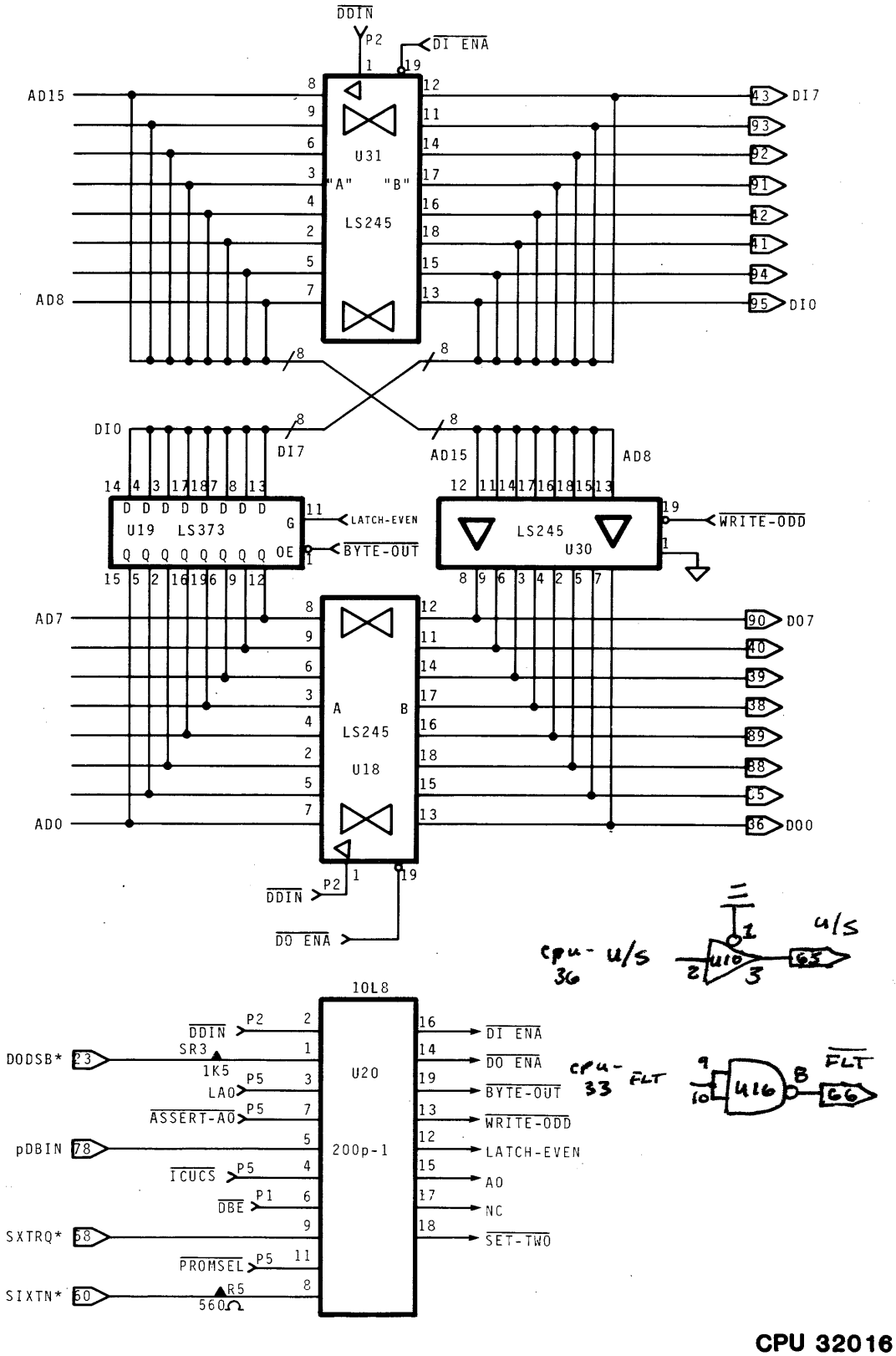

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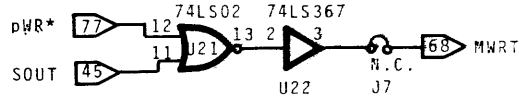

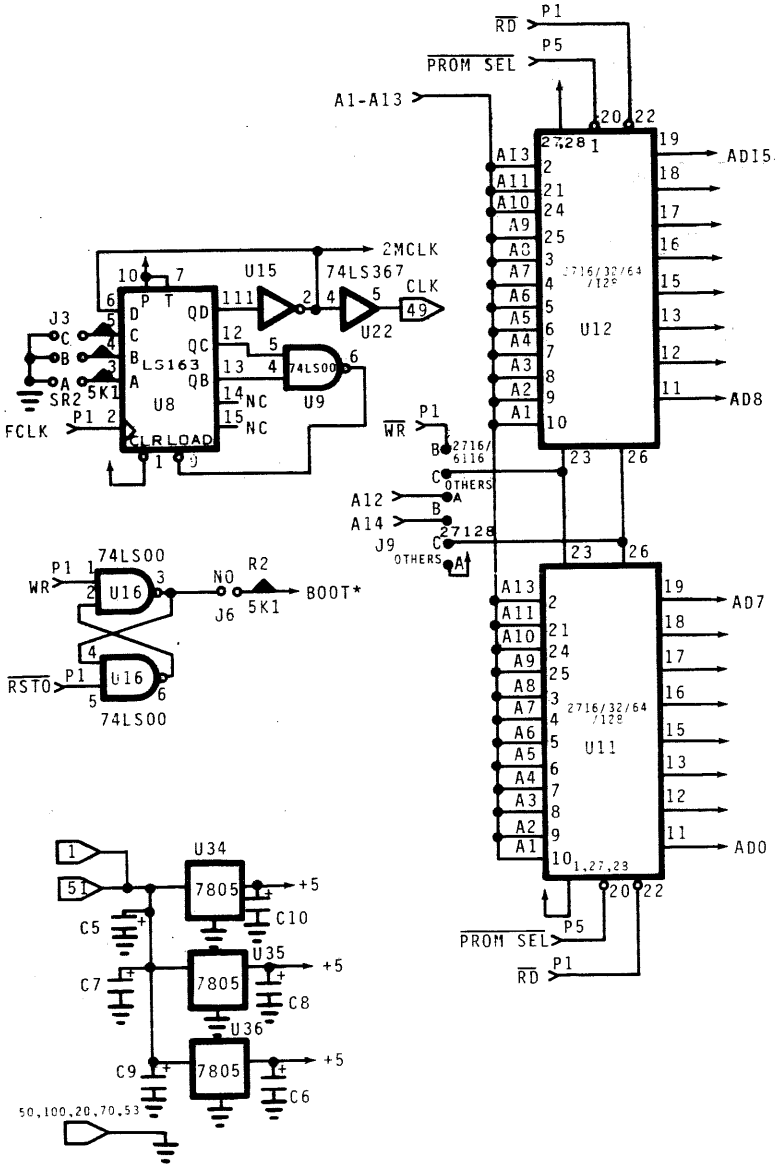

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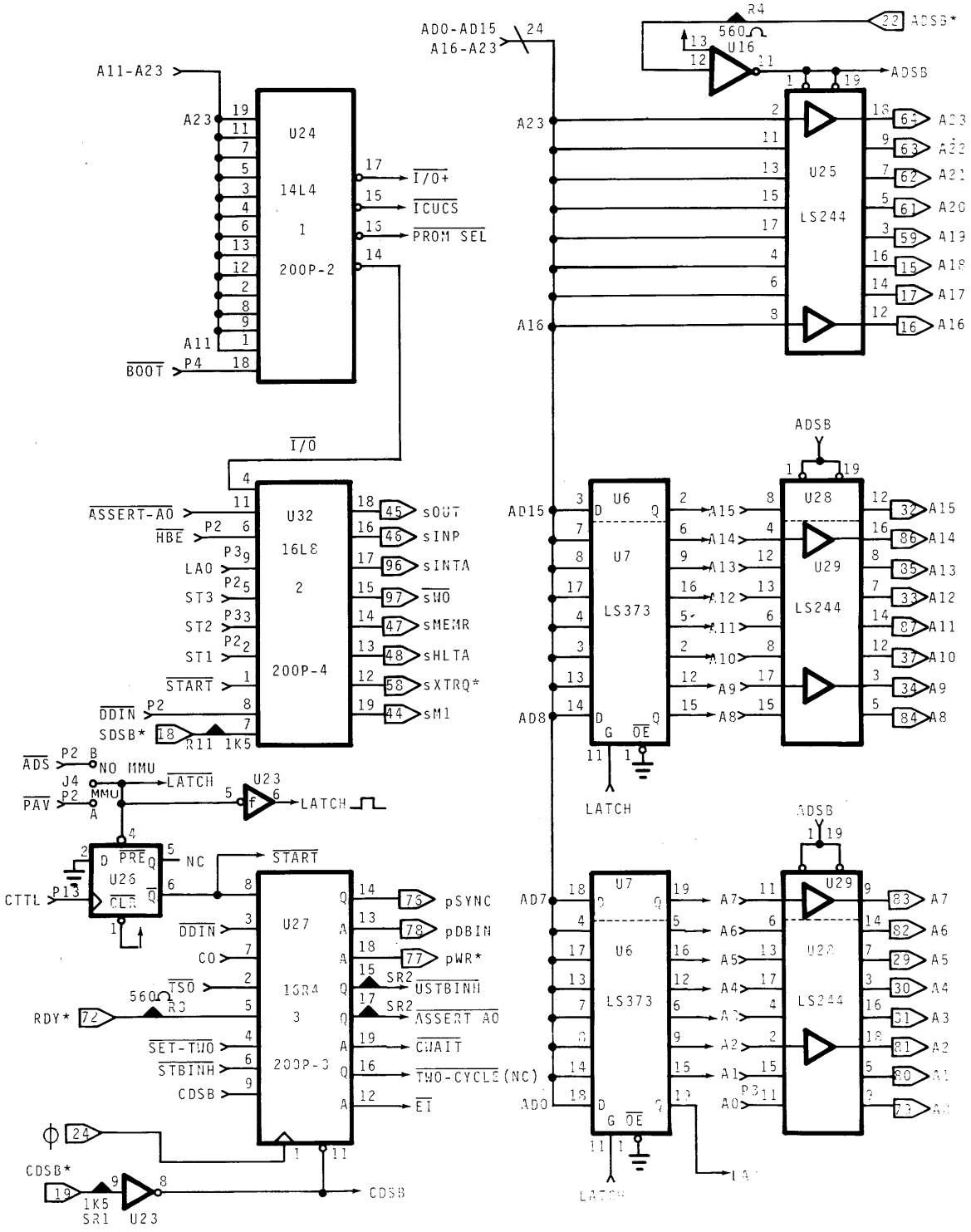

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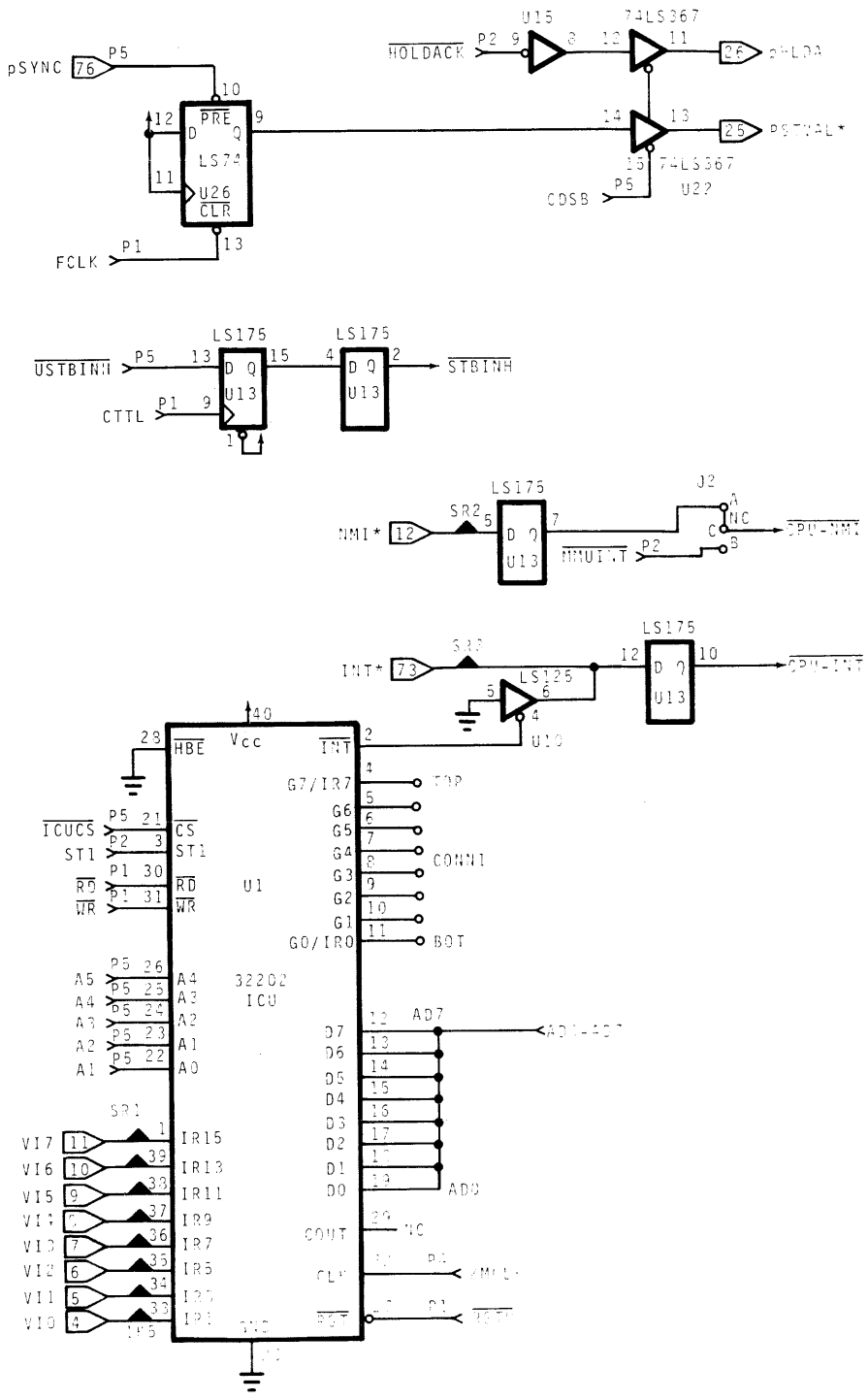

CPU 32016
200B

PARTS LIST

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Integrated Circuits

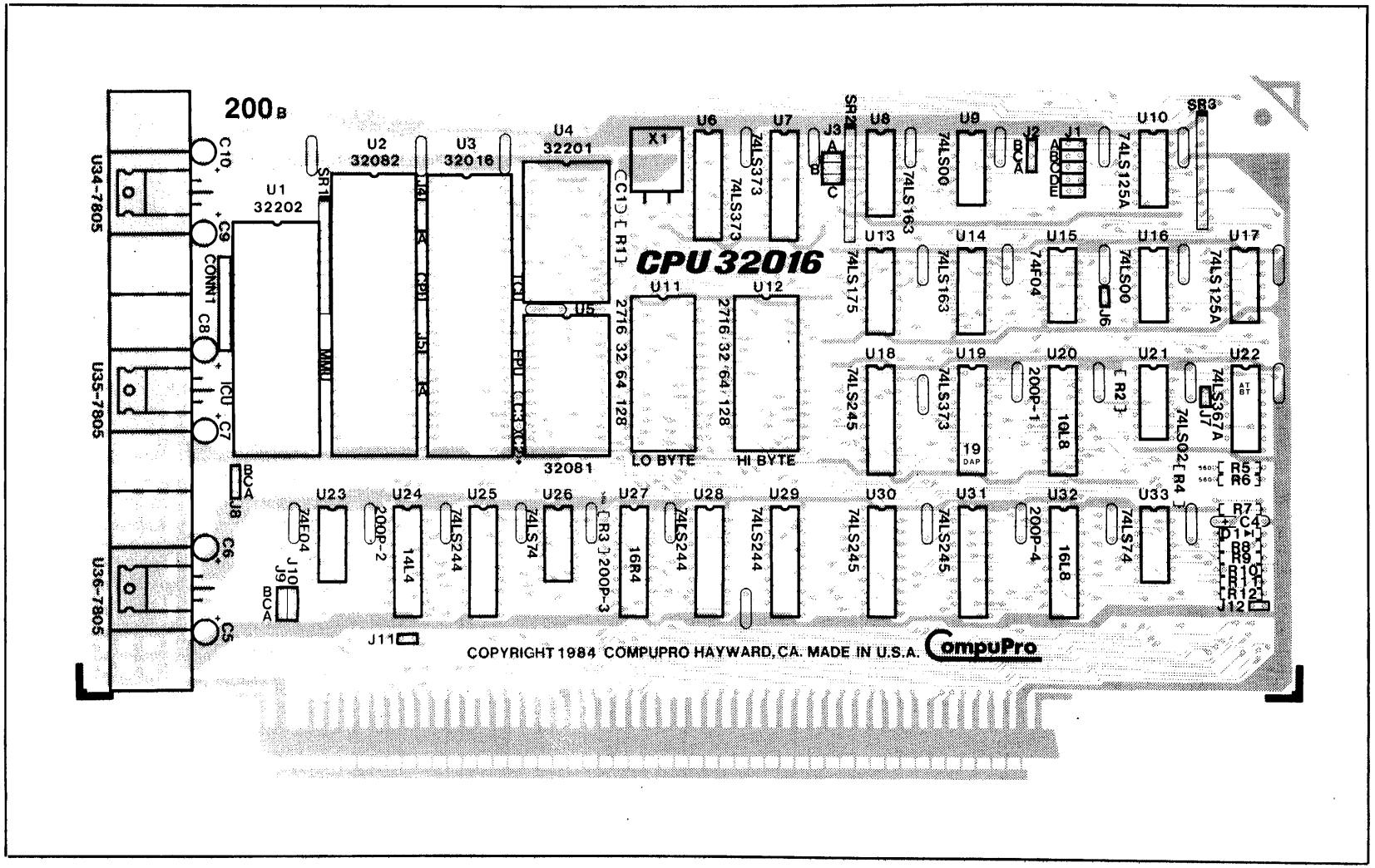
QTY	Description	
2	74LS00	Quad 2 input NAND (U9,U16)
1	74LS02	Quad 2 input NOR (U21)
2	74F04	Hex Inverter, fast (U15,U23)
2	74LS74	Dual D Flip-flop (U26,U33)
2	74LS125A	Quad tri-state buffer (U10,U17)
2	74LS163	Four bit counter (U8,U14)
1	74LS175	Quad latch (U13)
3	74LS244	Octal tri-state buffer (U25,U28,U29)
3	74LS245	Octal Transceiver (U18,U30,U31)
1	74LS367A	Hex tri-state buffer (U22)
3	74LS373	Octal transparent latch (U6,U7,U19)
1	32202	Interrupt Control Unit (U1)
1	32082	Memory Management Unit (U2)
1	32016	Central Processing Unit (U3)
1	32201	Timing Control Unit (U4)
1	32081	Floating Point Unit (U5)
1	10L8	10 In, 8 Out PAL (U20/200P-1)
1	14L4	14 In, 4 Out PAL (U24/200P-2)
1	16R4	8 In, 8 Out Registered PAL (U27/200P-3)
1	16L8	8 In, 8 Out Tri-State PAL (U32/200P-4)
2	2716/128	2K to 16K x8 EPROM (U11,U12) (Optional)
3	7805	Positive 5 volt regulator (U34,U35,U36)

Other Electrical Components

3	Sip Resistor 1.5K ohms (SR1,SR2,SR3)
1	270 ohm resistor (R8)
1	510 ohm resistor (R1)
3	560 ohm resistor (R3,R4,R5,R6)
1	1.5K ohm resistor (R11)
1	2.7K ohm resistor (R9)
1	5.1K ohm resistor (R2,R7,R10,R12)
6	greater than 1.5 uF tantalum radial cap 10v (C5-C10)
1	greater than 10 uF tantalum radial cap 6v (C4)
1	30 pF ceramic cap (C1)
1	1.0 uF tantalum radial cap (C2)
1	0.01uF ceramic cap (C3)
31	bypass cap (all unmarked)
1	CPUx2 processor crystal (X2)
1	1N914 or equivalent diode (D1)

Mechanical Components

9	14 pin sockets
5	16 pin sockets
13	20 pin sockets
6	24 pin sockets
2	28 pin sockets
1	40 pin socket
1	5 Long Double row pins (J1)
1	3 Long Double row pins (J3)
6	3 Long Single row pins (J2,J4,J5,J8,J9,J10)
4	2 Long Single row pins (J6,J7,J11,J12)
6	Shunts
3	Heatsinks
3	6-32 x 3/8" screws
3	6-32 hex nut
3	6-32 lock washer
1	PCB #200B
2	card ejectors
1	technical manual



COMPONENT LAYOUT

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Note: This warranty supersedes all previous warranties, and all other warranties are now obsolete.